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FILTROS A CORRENTES CHAVEADAS DIGITALMENTE PROGRAMÁVEIS PARA BAIXA TENSÃO

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CURSO DE PÓS-GRADUAÇÃO EM ENGENHARIA ELÉTRICA

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'Esta Tese foi julgada adequada para obtenção do Título de Doutor em Engenharia Elétrica, Área de Concentração em *Circuitos e Instrumentação Eletrônica*, e aprovada em sua forma final pelo Curso de Pós-Graduação em Engenharia Elétrica da Universidade Federal de Santa Catarina.'

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FILTROS A CORRENTES CHAVEADAS DIGITALMENTE PROGRAMÁVEIS PARA BAIXA TENSÃO

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Palavras-chave: Circuitos integrados baixa tensão, circuitos a correntes chaveadas, circuitos analógicos CMOS, circuitos analógicos digitalmente programáveis, filtros com resposta impulsiva infinita (IIR) e finita (FIR).

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Neste trabalho são propostos e implementados filtros a correntes chaveadas (SI) digitalmente programáveis, simples e totalmente balanceados, em tecnologia CMOS para baixa tensão. As chaves operam com tensão constante, evitando o "gap" de condução e a dependência da injeção de cargas e do tempo de acomodação com o sinal. A programabilidade dos circuitos SI, obtida usando técnica de divisão de corrente, é realizável em menores áreas e com desempenho superior se comparada ao método convencional em SI e ao uso de arranjos de capacitores em circuitos a capacitores chaveados. Apresentamos o projeto de integradores SI de segunda geração, uma célula básica para filtros de resposta impulsiva infinita (IIR). Utilizando o integrador SI, foi realizado um bloco de segunda ordem onde a freqüência central e o fator de qualidade podem ser sintonizados independentemente. Projetamos um circuito de amostragem/retenção (S/H) a correntes chaveadas para 20 MS/s. Utilizando a estrutura circular de linha de atraso foi realizado um filtro de resposta impulsiva finita (FIR) de quatro coeficientes. Para o projeto do filtro FIR totalmente programável é proposto um novo método para implementação de coeficientes negativos o qual apresenta simplicidade no controle do bit de sinal e alta velocidade comparado com outros métodos. Finalmente, foi projetado e simulado um filtro FIR de oito coeficientes totalmente balanceado usando o circuito S/H proposto. A programabilidade do filtro projetado foi testada. O filtro FIR é adequado à equalização adaptativa em aplicações tais como circuitos de leitura para unidades de disco. Alguns dos circuitos propostos foram projetados e fabricados em tecnologia CMOS duplo polissilício e duplo metal de 0.8 μm.

UNIVERSIDADE FEDERAL DE SANTA CATARINA

CURSO DE PÓS-GRADUAÇÃO EM ENGENHARIA ELÉTRICA

Digitally Programmable Low-Voltage Switched-Current Filters

Thesis submitted to
Universidade Federal de Santa Catarina
as a partial fulfillment of the requirements
for the degree of Doctor in Electrical Engineering.

FATHI ABD EL-FATTAH FARAG AHMED ZID

Florianópolis, Julho 1999.

DIGITALLY PROGRAMMABLE LOW-VOLTAGE SWITCHED-CURRENT FILTERS

By

Fathi Abd El-Fattah Farag Ahmed Zid

' This thesis has been submitted for the degree of Ph. D. in Electrical Engineering and approved in its final form by the Graduate Course in Electrical Engineering, Federal University of Santa Catarina.'

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DIGITALLY PROGRAMMABLE LOW-VOLTAGE SWITCHED-CURRENT FILTERS

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In this work, single-ended and fully balanced digitally programmable low-voltage (LV) complementary metal-oxide-semiconductor (CMOS) switched-current (SI) filters are proposed and implemented. The switches operate at constant voltage thus avoiding the conduction gap as well as the signal dependence of both charge injection and settling time. The programmability of the filters is achieved using the current division technique. The programmability is realized in small area and with excellent performance if compared to conventional SI programming methods and to the use of capacitor array in switched-capacitor circuits.

We show the design of a second generation SI integrator, a basic cell for IIR filters. A programmable second order section has been realized using the proposed integrator. The center frequency and quality factor can be tuned independently.

A programmable switched-current sample-hold (S/H) circuit has been designed for 20M sample/s. A single-ended 4-tap finite impulse response (FIR) filter has been realized using the circular delay line structure. For a fully programmable FIR filter design, a new method for the implementation of negative coefficients is proposed which achieves simplicity in sign-bit control and high-speed compared with other methods. Finally, a fully balanced 8-tap FIR filter has been designed and simulated using the proposed S/H circuit. The programmability of the designed filter has been tested. The FIR filter is suitable for adaptive equalization such as in disk-drive applications.

Some of the proposed circuits have been designed and fabricated in a 0.8 μm double poly-silicon double-metal CMOS technology.

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Fathi Abdel-Fattah .Farag

To

my wife Sahar

and

sons

Khaled and Moumen

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PREFACE

This thesis is concerned with digitally programmable switched-current technique suitable for low voltage power supply. Programmable single-ended and fully balanced filter (IIR and FIR) blocks are designed and tested. The programmability of the switched-current circuits is achieved by using the current division technique. The thesis is organized as follows.

In the first chapter, we review some key limitations in analog circuit design at low power supply voltage.

In Chapter 2, the conventional switched-current technique is briefly reviewed. It is shown that the conduction gap problem for the conventional SI technique at low voltage operation is much the same as for the standard SC technique. Finally, a new SI technique that has been used in this work is reviewed.

In Chapter 3, a second generation SI integrator is proposed. A programmable integrator-based biquad, which allows independent tuning of the center frequency and the quality factor has been implemented.

Chapter 4 is dedicated to the analysis and design of programmable single-ended and fully balanced SI sample-hold circuits for 20 MHz sampling rate.

Chapter 5 is dedicated to the design and simulation of a finite impulse response (FIR) filter. The circulating form realization of the FIR filters (single-ended and fully balanced) is used to reduce the multiple re-sampling errors.

In Chapter 6, a description of the layout of some circuits designed during the preparation of this work together with experimental results is presented.

CHAPTER 1

LOW-VOLTAGE ANALOG DESIGN

1.1 INTRODUCTION

Recently, the power supply voltage for many commercial very large scale integrated (VLSI) circuits has been decreased to 3V and will continue to decrease to further lower levels. This trend [1, 2] is driven by three main factors :

- The scaling of VLSI technologies (deep-submicron).
- Power management in large VLSI chips.
- Increased market demands for mobile or portable battery-operated products.

These factors are technology, design and market-driven respectively, and as such seem independent of one another. However, they are to a large extent interrelated.

Obviously, minimum feature sizes are scaled down in three dimensions. At the present time, VLSI technologies are characterized by channel lengths in the range from 0.5μm to 0.25μm. By convention the channel length of the MOS transistors is used as the reference length. Scaling is one effective method of reducing the cost of IC products, i.e. more components are integrated on a single chip with roughly the same effort and cost. In addition, smaller geometry, in general, lowers the parasitic capacitances and increases transconductance in MOS devices, yielding higher-speed circuits. However, scaling inevitably results in thinner MOS gate oxide. Hence, scaled down devices are subject to breakdown at relatively low voltages because of the increase in electric field. Therefore, the reduction of the supply voltage is necessary.

With the reduction of the supply voltage, analog designers are faced with new problems in circuit design. Key design issues in low supply voltage must be addressed to maintain the same system performance achieved with relatively high supply voltage. Actually, in analog circuit design, supply voltage reduction is a primary factor of circuit modifications.

The design at low supply voltages is particularly harder in mixed mode VLSI signal processing systems [3, 4], in which analog and digital circuits are integrated on a single chip. The electrical parameters of transistors are optimized for digital circuits due to the fact that they usually account for the majority of the total chip area. For instance, as the technological process scales down, the MOSFET threshold voltage remains about the same. The reduction of the threshold voltage that would be necessary for analog circuits usually produces two negative effects on digital circuits, the reduction of noise margin and high leakage currents. Of course it might be possible to use multi-threshold voltage process technology in which a high threshold voltage can be used for digital circuits and a low threshold voltage can be used for analog circuits (continuous-time and sampled-data circuits) [5]. This solution, however, increases the cost of IC products.

Digital circuits do not suffer significantly under low voltage conditions and can perform well with slight modifications, while new analog techniques for low voltage circuits must be developed. Furthermore, in digital design lowering the supply voltage implies in lower power consumption whereas in analog design a lower supply is not a necessary neither sufficient condition for low power. In fact, lowering the supply may or may not reduce power consumption depending on whether certain design changes are made to maintain or restore the analog performance at acceptable levels. In analog circuit, the power consumption per pole is in a crude approximation proportional to the dynamic range (DR) [6, 7, 8]:

$$P = \eta kTf_o(DR) \tag{1.1}$$

where DR is defined as the ratio of the mean square value of the signal to the mean square value of the noise, f_o is the filter pole frequency, η is a dimensionless factor depending on the implementation of the filter and kT is the thermal energy. Equation (1.1) is derived neglecting the bias currents of the amplifiers, assuming a pure capacitive load C and that the only contribution to noise is thermal noise. Here, we consider the mean square voltage noise at the load to be equal to kT/C. Consequently, to keep the same DR, the load capacitor should be scaled up with the square of the supply voltage scaling factor. In this idealized situation, for a given dynamic range, the power consumption is independent of the supply voltage. In practice, however, power dissipation is generally dominated by the static dissipation of the amplifier. As shown in [9], to keep the same circuit performance (signal-to-noise ratio and bandwidth), the static power consumption is increased for lower supply voltages.

In this chapter, we will review some key limitations in analog circuit design at low-voltage power supply. Some solutions based on both integrated circuit technologies and circuit design strategies are mentioned.

1.2 LIMITATIONS OF LOW-VOLTAGE OPERATION

The operational amplifier is a widely used building block in analog circuits. The power supply voltage must be higher than a minimum value to allow for correct operation of the amplifier. Fig.1.1 shows the most simple input and output stages of operational amplifiers. For the input, the maximum bias voltage V_B is around V_{DD}-(V_{Top}+V_{DSsat}). Another boundary is set by the output stage; the minimum supply voltage [10] is approximated as

$$V_{DD,\,min} \cong V_{DSsat,n} + V_{swing} + V_{DSsat,p} \tag{1.2}$$

Consequently, low supply voltage causes directly shrinking of both the voltage swing and the dynamic range.

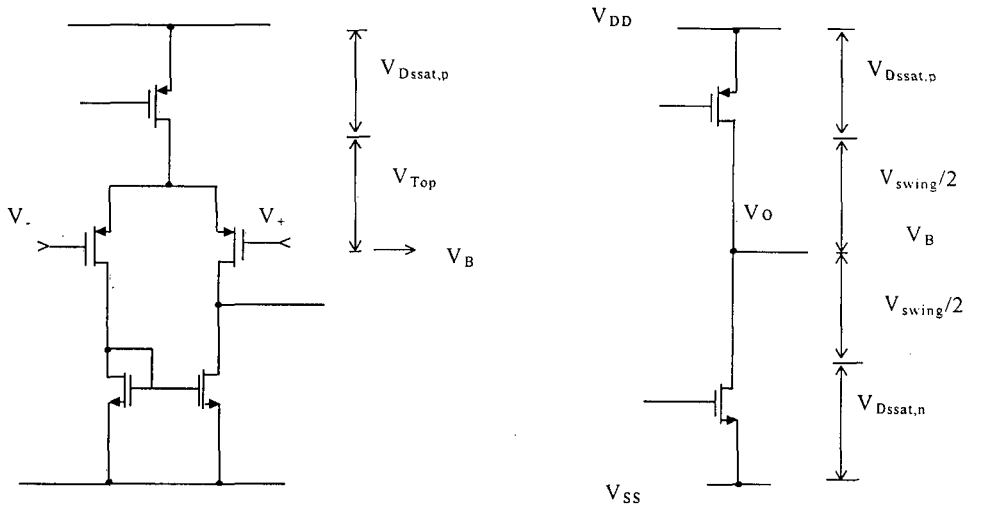


Fig. 1.1. The common-mode input range and output range of an op-amp.

Another problem that must be faced at low-voltage is related to the switch. The complementary MOS switch has been largely employed in sampled-data (switched-capacitor (SC) and switched-current) circuits. Fig. 1.2 shows an S/H circuit. Around $V_S=V_D=V_{in,}$ in strong inversion (see Appendix A),

$$g_{DSn} = \mu_n C'_{ox} \frac{W}{L}(V_{DD} - V_{Ton} - nV_{in}) \tag{1.3}$$

The expression for the conductance g_{DSp} of the p-channel transistor is similar to (1.3).

The switch conductance is dependent of both the supply voltage and the input signal. Fig. 1.3 illustrates the rail-to-rail operation of the CMOS switch. Note the dependence of the total switch conductance ($G_{on}=g_{DSn}+g_{DSp}$) on the input signal. Reducing the supply voltage reduces the overdrive voltage of the MOS switches. Consequently, the overlapping conduction range of the nMOS and the pMOS devices is reduced. When

the supply voltage reaches $(V_{Ton}+|V_{Top}|)/(2-n)$, the on-resistance becomes very large and the rail-to-rail operation is not practical any more. In conclusion, the conduction gap is one of the most significant obstacles for low-voltage operation in sampled-data circuits.

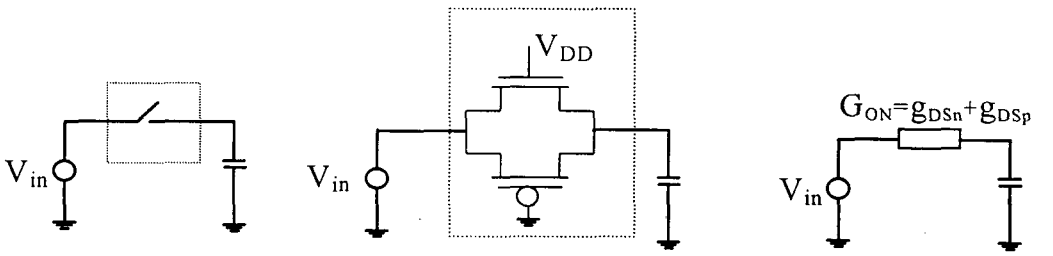
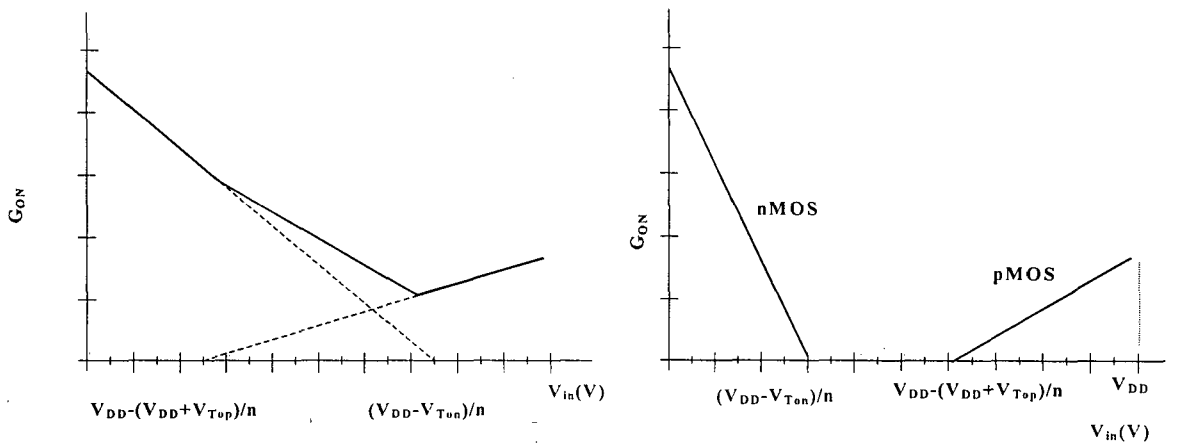


Fig.1.2. The sample-hold circuit.

(a) Basic sample-hold scheme.

(b) Basic sample-hold and the CMOS switch.

(c) Basic sample-hold and the on-conductance of the CMOS switch.



V_{DD} =5V V_{DD}=1.5 V

Fig.1.3. On-conductance of a CMOS switch for V_{DD}=5V and 1.5V.

1.3 LOW-VOLTAGE CIRCUIT DESIGN TECHNIQUES

In this section, we describe two existing solutions that allow for low-voltage operation of CMOS switches. The first is based on a special multi-threshold process, and the second is based on circuit design techniques.

1.3.1 TECHNOLOGY CONSIDERATIONS FOR LOW-VOLTAGE ANALOG CIRCUITS

As mentioned above, low supply voltage has generated design problems such as reduction of the dynamic range and the difficulty of turning on the CMOS/MOS switches over the entire voltage swing. From the technology side, special techniques to overcome these problems exist. One is enlarging V_{swing} by using a dedicated process, which has a special low V_T nMOS transistor [11, 12]. In [11] an extra nMOS transistor with V_{Ton} =0.2V is used as a switch, which allows a 1V voltage swing from 1.4V power supply.

A less expensive alternative is to use a technology that provides unimplanted devices. In this technology, a low threshold nMOS is realized by a shielding technique [8]. The resulting nMOS device has a typical threshold of 300mV with a relatively small body effect. Other possible solution is the use of bipolar devices of BiCMOS technology [13, 14].

Technology solutions to solve problems of low-voltage circuits are expensive. Thus, circuit designers have developed solutions based on the circuit art that will be reviewed in the next section.

1.3.2 DESIGN STRATEGY FOR LOW-VOLTAGE CIRCUITS

Analog circuit designers have introduced circuit cells appropriate for low-voltage operation [10, 15] to avoid the expensive multi-threshold technique. A general guideline for the design of high gain amplifiers at low-voltage is the use of multistage cascade structures instead of stacked transistors. Moreover, for large voltage swing, the output stage must achieve rail-to-rail swing. Details about low-voltage op-amp design can be found in [8, 16].

This work concentrates on circuit techniques that circumvent the problem of the conduction gap of the switches. One manner to overcome the switch gap problem is the clock multiplication technique [17]. In this method, a higher voltage for driving the critical switches (switches connected to non-constant voltage) is generated on-chip from the low power supply. This technique generates problems such as the possibility to create latch-up. Furthermore, the use of higher voltages is not allowed anymore in advanced sub-micron CMOS technologies due to reliability considerations [10].

Another approach to allow for proper operation of switches in low-voltage SC circuits is the switched-opamp technique [10, 18]. In this technique, the critical switch is eliminated, and its function is realized by turning on and off the operational amplifier attached to this switch. Fig.1.4 shows the conventional SC circuit and the switched op-amp equivalent circuit. This technique is based on the switched op-amp output to be in a high impedance state during the low state of the clock, as shown in Fig. 1.4 (c).

In the switched-opamp technique, the maximum sampling frequency is limited by the time necessary to turn on and off the op-amp which is limited to a few hundred kHz [8]. The seminal switched op-amp technique described in [10] has been slightly modified in [18] to allow rail-to-rail output swing.

From the discussion above, the ideal solution to the conduction gap is that all switches operate at a constant voltage level that is out of the conduction gap.

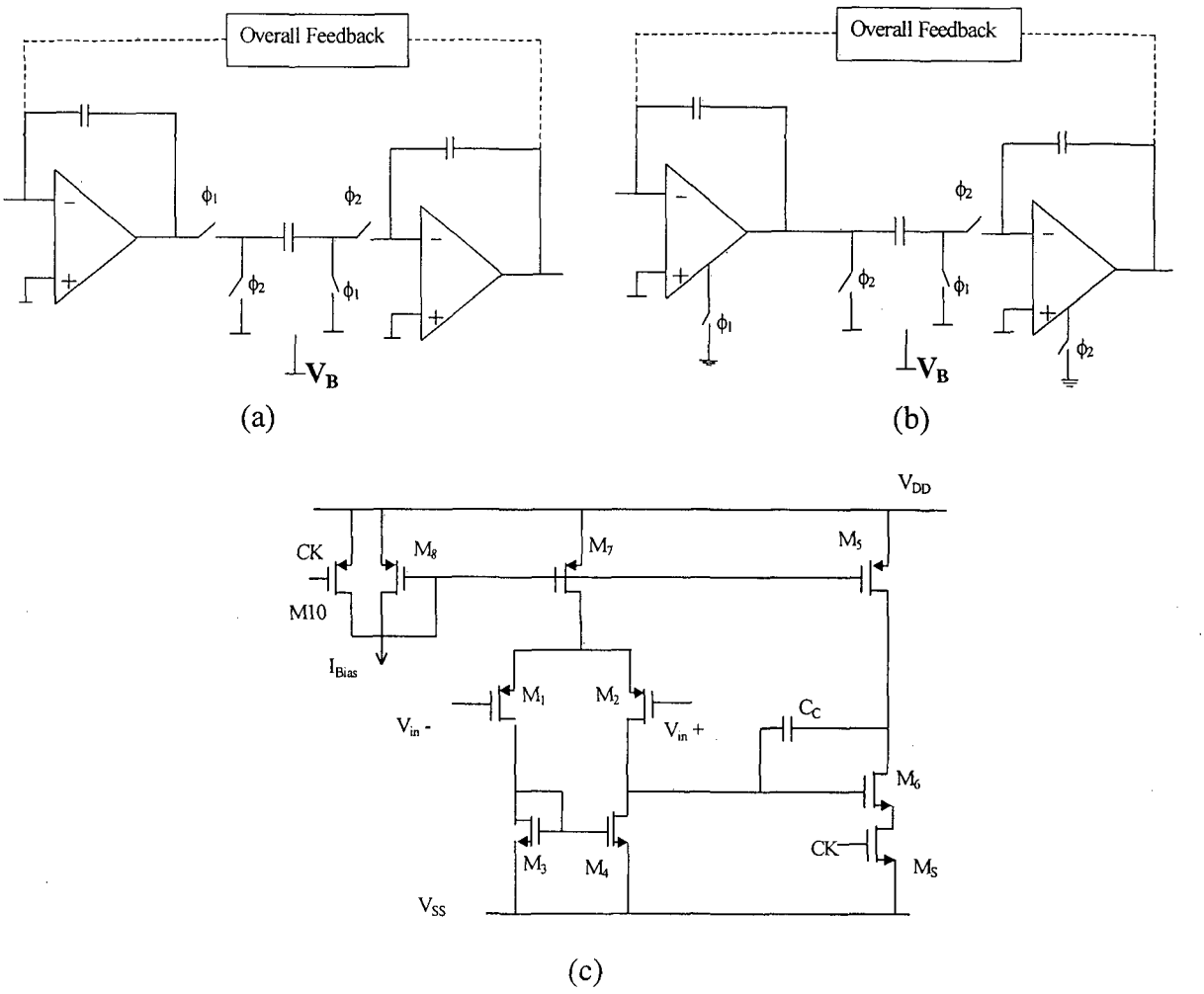


Fig.1.4. Switched-opamp technique [10].

(a) Conventional SC integrator.

(b) Switched-opamp equivalent SC circuit.

(c) Switched-opamp.

CHAPTER 2

SWITCHED-CURRENT TECHNIQUES AND LOW-VOLTAGE OPERATION

2.1 INTRODUCTION

Sampled-data circuits have been intensively employed in VLSI chips. The switched-capacitor (SC) technique has been the prevailing one over the last two decades. Using MOS amplifiers, switches, and precision linear capacitors, SC filters achieve high accuracy with low distortion. The basic building block of SC circuits is the sampled-data integrator in Fig. 1.4. (a).

In the late 1980s, a new sampled-data technique called switched-current (SI) was introduced [19, 20]. The major advantage of the SI technique compared to the SC technique is the compatibility with standard digital VLSI processes, because it does not need linear capacitors. In this chapter, the conventional switched-current technique is briefly reviewed. It is shown that the conduction gap problem for the conventional SI at low voltage operation is much the same as for the standard SC technique. Finally, a new SI technique that has been proposed in [21] is reviewed.

2.2 CONVENTIONAL SWITCHED-CURRENT (SI) TECHNIQUE

2.2.1 BASIC OPERATION

Generally, current-mode signal-processing circuits employ the current mirror as their main block. The conventional current mirror is based on matching properties of

transistors. Ideally, the drain current (I_D) of the MOS transistor working in saturation [22] can be described in terms of the terminal voltages as

$$I_D = \left(\frac{W}{L}\right)\{f(V_G, V_S)\} \tag{2.1}$$

where W is channel width, L is channel length of MOS transistor, V_G, V_S are the gate and source potentials referred to the substrate.

From (2.1), two matched MOS transistors biased in saturation with the same gate and source potentials have ideally the same drain current if their aspect ratios (W/L's) are equal. In the current mirror illustrated in Fig. 2.1.(a), the current enters in a diode-connected MOS transistor (master) to generate a terminal voltage (V_g) that depends on the input current (i_{in}). The resulting voltage, V_g, forces the second transistor (mirror) to draw the same current as the first one.

The basic cell of conventional SI circuits is the current mode sample-hold (S/H) [19] depicted in Fig. 2.1.(b). In this figure, transistor M_1 operates in saturation and the output voltage is assumed to drive M_2 into saturation also. The input current is stored as a voltage across the gate capacitor of M_1. When switch M_s is closed, the drain currents of M_1 and M_2 are equal, that is, the output current follows the input current (sample). After switch M_s is open, the drain current of M_2 (i_{d2}) is held constant at its previous value. The circuit shown in Fig. 2.2.(b) is a half delay cell and all conventional SI circuits are derived from it.

The basic SI S/H suffers from certain limitations, such as mismatch between the MOS transistors, finite output impedance and charge injection from the switches. All these error sources limit the accuracy of the sample-hold circuit.

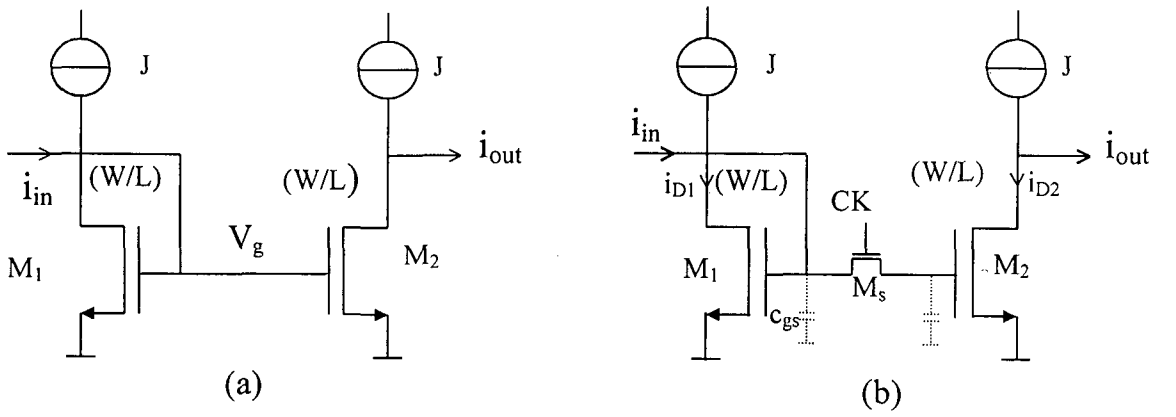


Fig. 2.1. Basic block for current mode signal processing.

(a) Simple current mirror.

(b) Conventional S/H circuit.

The device mismatching is due to the gradual variation during chip fabrication (more details about this subject can be found in chapter 6) and is a common problem in analog integrated circuits. Mismatch can be minimized using special layout techniques. In the SI technique, the dynamic current mirror (current copier) [23, 24] has been proposed to avoid errors due to mismatch because it uses only one MOS transistor to realize the S/H, as shown in Fig. 2.2.(a). Furthermore, the silicon area and the power consumption have been ideally reduced by 50% compared with the simple technique. Fig. 2.2.(a), illustrates dynamic current mirrors controlled by a two-phase clock.

The non-ideal input/output impedances causes errors in current gain in case of two cells in cascade. In a simple current mirror, the typical current gain error is around 1% [25]. To improve the accuracy, the cascode current mirror technique can be used [26]. The cascode SI cell schematic is illustrated in Fig. 2.2. (b). Also, the active current mirror shown in Fig. 2.3.(a) has been used [27, 28] to reduce the effects of the finite output impedance.

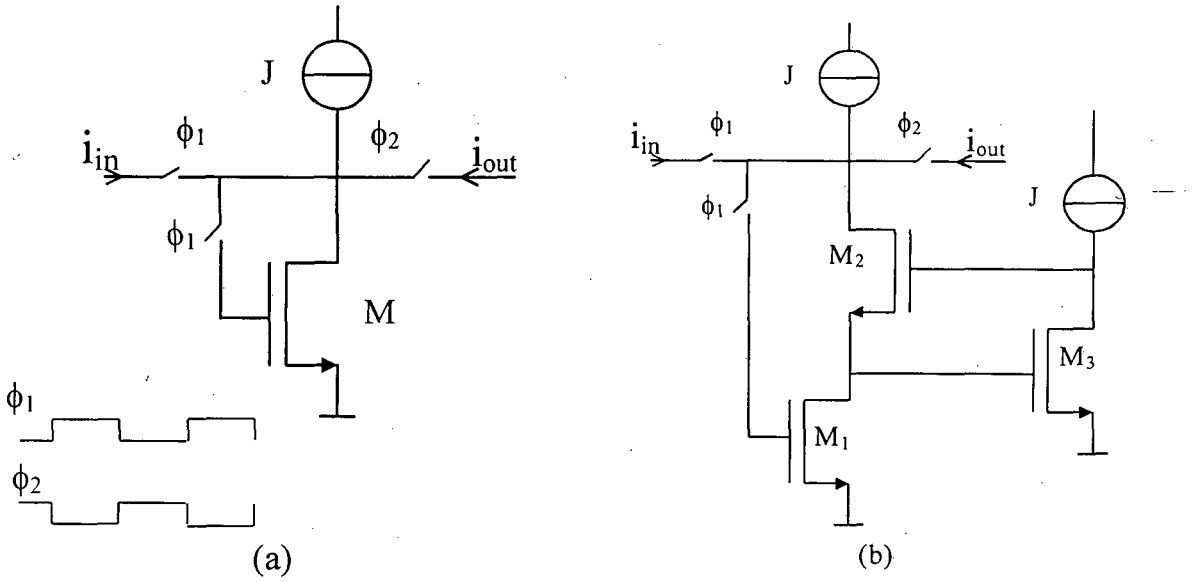


Fig. 2.2. Switched-current sample-hold circuits -I.

(a) Current copier.

(b) Regulated cascode.

Another error source in SI circuits is the charge injected into the holding capacitor during transition of the switch from on to off. This charge results from both the overlap capacitance between gate and the switch terminal to which the holding capacitance is connected and from the channel charge released when the transistor turns off. A portion of the charge injected (ΔQ) into the holding capacitor (C_G) during the switching off process changes the gate voltage by ΔV_G. This gate voltage changing produces an error in the drain current

$$\Delta i \approx g_m \Delta Q / C_G \tag{2.2}$$

Thus, a high value of C_G, a minimum size switch, or some compensation technique must be used to minimize the charge injection effect.

A common technique used in SC circuits for compensation of the charge injection effect is the dummy MOS switch. Several other techniques, such as the one shown in [25], have been proposed for reducing the effects of charging injection in SI circuits.

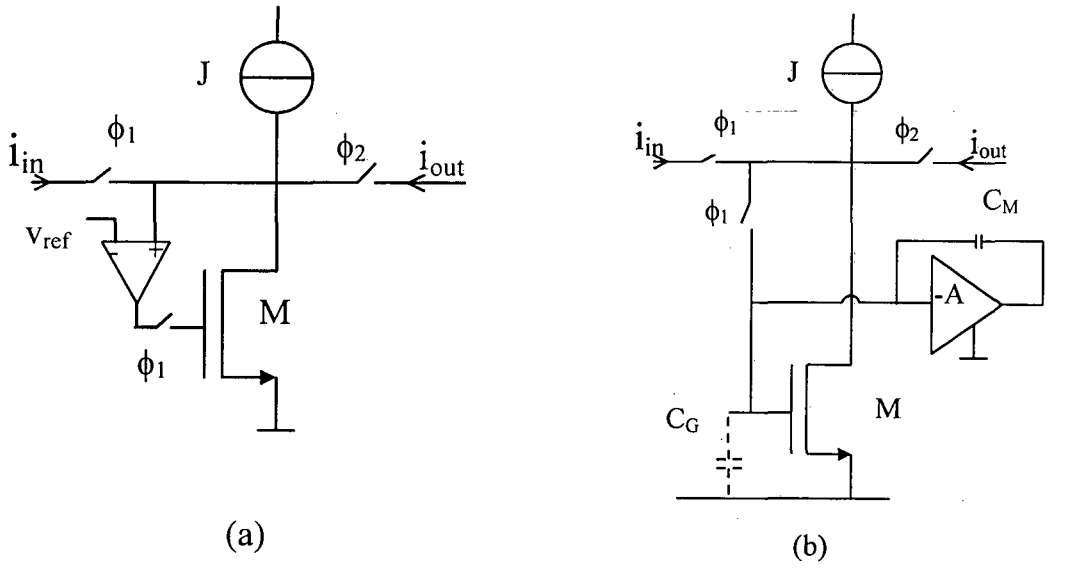


Fig. 2.3. Switched-current sample-hold circuits-II.

(a) SI sampler with active-negative feedback.

(b) Miller-enhanced memory cell.

The dummy transistor with the Miller enhancement method has been proposed in [29] to reduce the effect of charge injection. This method simulates a large capacitor using the Miller effect as shown in Fig. 2.3. (b). The total gate capacitance becomes $(A+1)C_M+C_G$, therefore reducing the charge injection effect (equation 2.2).

2.2.2 FIRST AND SECOND GENERATION INTEGRATORS

The conventional SI technique presents two integrator architectures [19, 20]. The first generation SI integrator [19], depicted in Fig. 2.4. (a), is composed of two cascaded sample-hold circuits and a feedback path. The first generation integrator suffers from mismatch error and high current consumption.

The second generation SI integrator [20] is illustrated in Fig. 2.4. (b). It is constructed of two dynamic current mirror cells in cascade. The most important advantages of the second generation integrator compared to the first generation integrator are insensitivity to mismatch and small current consumption. The switching

sequence shown in Fig. 2.4.(c) is necessary to avoid the loss of information during clock transition in a practical implementation. The input/output transfer function is given by

$$\frac{I_0^{\phi_1}(z)}{I_{in}^{\phi_1}(z)} = A_1 \frac{z^{-1}}{1-\beta z^{-1}} \tag{2.3}$$

where $A_1 = \alpha_1/(1+\alpha_2)$ and $\beta = 1/(1+\alpha_2)$.

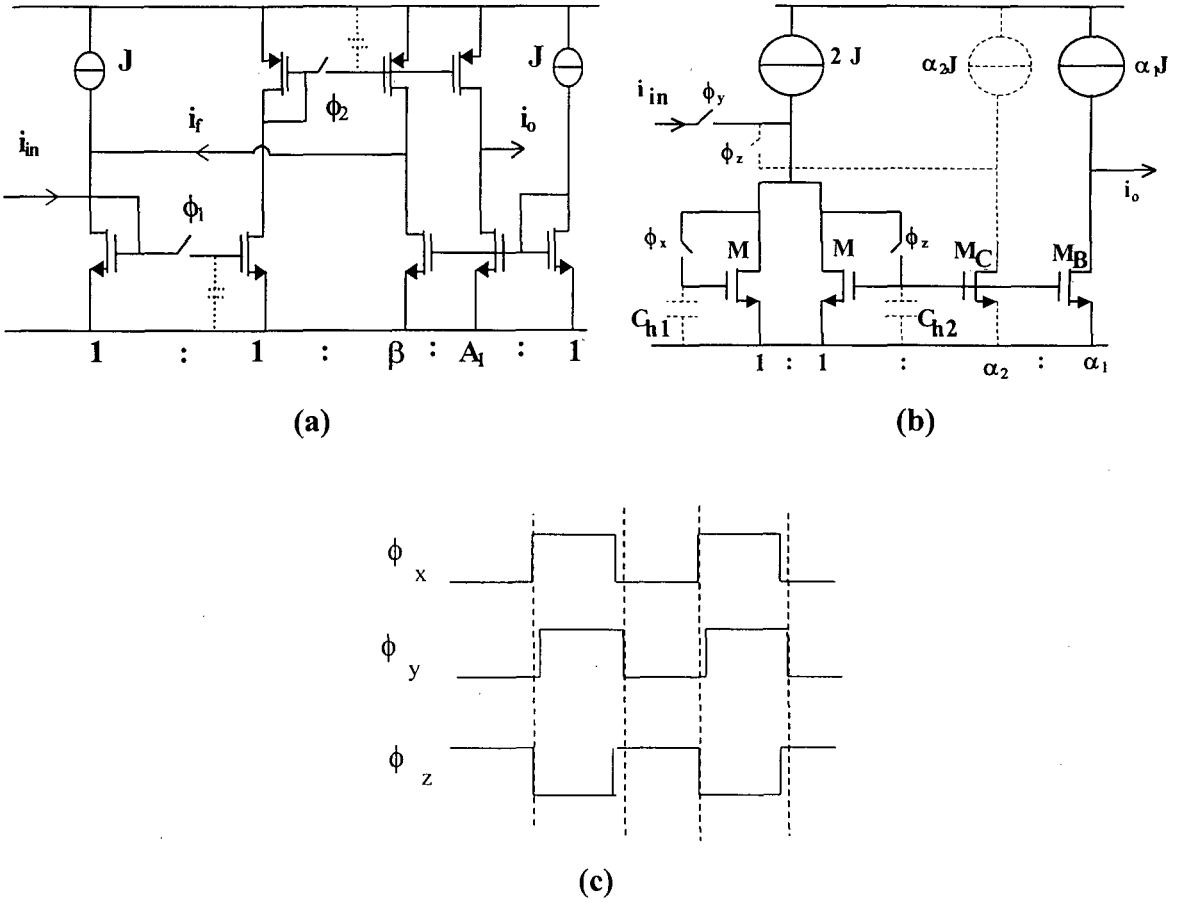


Fig. 2.4. Conventional switched-current integrators.

(a) First generation SI integrator.

(b) Second generation SI integrator.

(c) Clock phases.

2.2.3 LOW-VOLTAGE OPERATION

Each switch in conventional SI circuits operates at a signal dependent voltage as can be seen in Figs. 2.1 and 2.2. Thus, for low voltage operation, each switch is susceptible to the conduction gap [10]. Therefore, conventional SI circuits, like standard SC circuits, are not suitable for low-voltage operation.

For proper operation, the output voltage of the current copier (Fig. 2.2.a) is limited by the drain-source saturation voltage of the transistor and by a maximum critical voltage (V_{crit}) related to the maximum allowable settling time. V_{crit} should not be larger than a certain value that would ensure a minimum on-conductance of the n-MOS switch. At low supply voltage , the biasing current J must be adjusted to force the output voltage to be within this voltage range. Note that both the on-conductance and the channel charge of the n-MOS switch are dependent of the signal level. Consequently, charge injection becomes signal-dependent, and thus difficult to compensate.

2.3 NEW METHODOLOGY FOR LOW-VOLTAGE

2.3.1 DELAY/AMPLIFIER CELL

Recently a new SI technique has been developed in [21]. The basic cell in this method is the current mirror circuit shown in Fig. 2.5. (a). Assuming that the operational amplifier is ideal, transistors M_1 and M_2 are both biased with the same set of voltages. Neglecting transistor mismatch, we obtain:

$$i_o = -[(W/L)_{M2}/(W/L)_{M1}]\ i_{in} \qquad (2.4)$$

Therefore, the output current i_o is an inverted replica of the input current i_{in}.

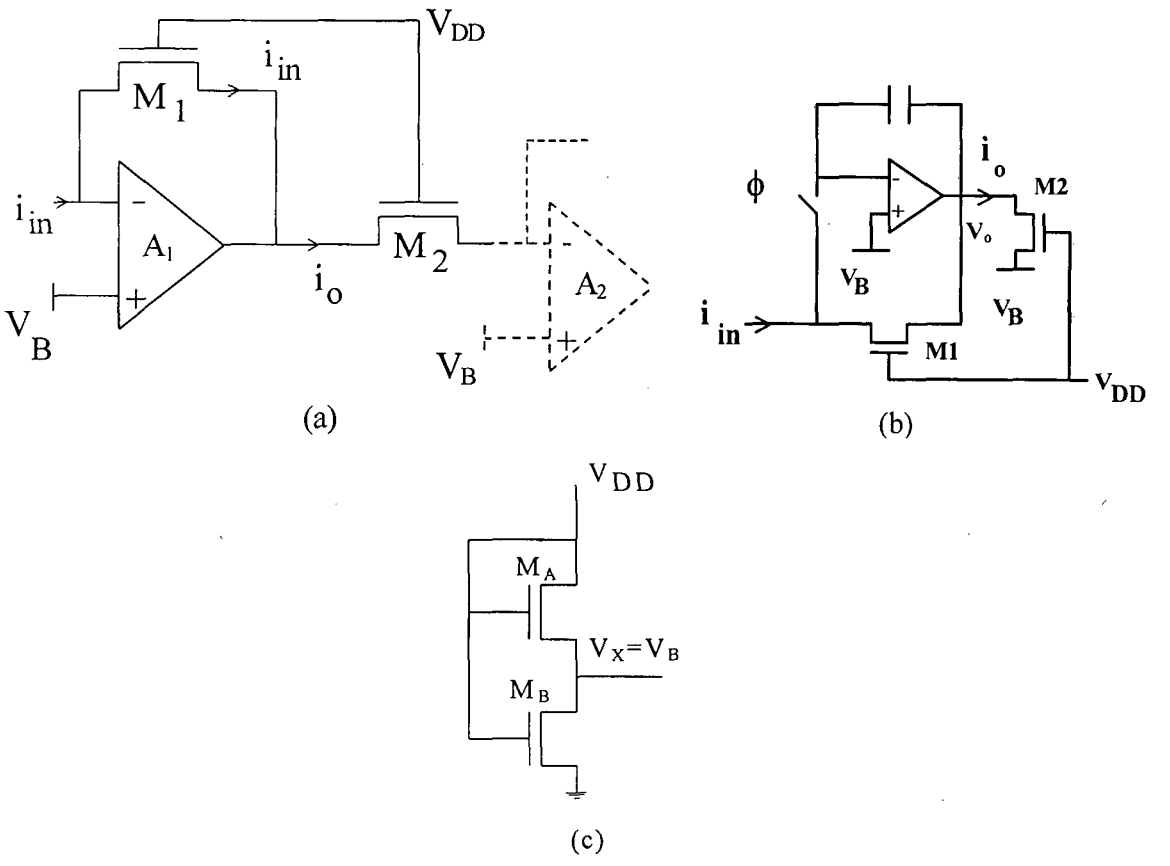


Fig. 2.5. The basic cells of the switched-current technique [21].

(a) Current mirror.

(b) Switched-current S/H block.

(c) The bias voltage generation.

Based on this current mirror, the sample-hold circuit illustrated in Fig. 2.5.(b) was proposed in [21]. The circuit operates as follows :

1. When the switch is closed, the hold capacitor is charged to a voltage V whose value depends on the input current i_{in}, the transistor parameters, and the gate voltage. The output current is such that $i_o = -\beta i_{in}$, where $\beta = (W/L)_{M2}/(W/L)_{M1}$.
2. When the switch opens, a voltage equal to V is held on the capacitor and the current is sustained at the output.

An important property of the proposed current mirror is that the switches operate at a constant voltage V_B provided by the bias circuit shown in Fig. 2.5. (c). Therefore, the

conduction gap [8, 10] of the switches at low power supply voltages is avoided. Furthermore, the holding capacitor is not necessarily a linear capacitor. Also, the charge injected during turn-off is signal-independent, which improves the accuracy of the S/H circuit.

An appropriate choice of the bias voltage (V_B) allows for the highest current swing. Fig. 2.5.(c) illustrates the bias voltage generation [21, 30]. M_A and M_B are identical transistors. Thus, V_x (V_B) can be calculated as:

$$V_X = V_P(1 - 1/\sqrt{2}) \tag{2.5}$$

where $V_P = (V_G - V_{Ton})/n$ is the pinch-off voltage [30,31], V_G is the gate-to-bulk voltage, V_{Ton} is the threshold voltage and n is the slope factor.

2.3.2 ANALOG ERRORS IN A CURRENT MIRROR [21 , 32]

2.3.2.1 Op-amp finite gain

The finite gain of the op amp of Fig. 2.5. (a) causes an error in the current gain equal to

$$\varepsilon = \frac{-1}{A_{vo}}\left\{\frac{g_{ms1}}{g_o}\left(1 + A_i\right) + 1\right\} \tag{2.6}$$

where A_{vo} is DC open-loop gain of the op amp, g_{ms1} is the source transconductance of M_1, g_o is output conductance of the op amp and A_i is the current gain.

2.3.2.2 Op-amp finite bandwidth

The bandwidth of the current mirror in Fig. 2.5. (a) is determined by the op-amp gain-bandwidth product provided that the intrinsic cutoff frequencies of M_1 and M_2 are higher than the op amp gain-bandwidth product.

2.3.2.3 Op-amp offset voltage

A difference (ΔV_{OS}) between the offset voltages of the op-amps (A_1 and A_2) in Fig. 2.5.(a) gives rise to a DC error Δi_o in the output current given by

$$\frac{\Delta i_o}{i_{o\max}} = 2\sqrt{2}\frac{\Delta V_{OS}}{V_P} \tag{2.7.a}$$

where

$$i_{o\max} = \frac{\beta_2 n}{4} V_P^2 \tag{2.7.b}$$

2.3.2.4 Transistor mismatch

A difference in the transconductance parameters produces a relative gain error proportional to the mismatch in the transconductance parameters. A mismatch in the threshold (pinch-off) voltage causes gain error and harmonic distortion, summarized by the following expression:

$$x_2 = \left(1 + \frac{\Delta V_P}{V_P}\right) x_1 + \frac{\Delta V_P}{V_P}\left(\frac{x_1^2}{8} + \frac{x_1^3}{32} + ..\right) \tag{2.8}$$

where $\frac{\Delta V_P}{V_P} = \frac{\Delta V_{TO}}{V_{DD} - V_{TO}}$ is the threshold voltage mismatch normalized to the overdrive voltage and $x_1 = i_{in}/i_{in\max}, x_2 = i_o/i_{o\max}$ are the normalized input and output currents.

2.3.2.5 Noise

The noise component of the output current is due to the op-amp noise, the noise generated by transistors M_1 and M_2 as well as the input noise. The mean square value of the output current noise component is given by

$$\overline{i_o^2} = \left(\frac{g_{ms2}}{g_{ms1}}\right)^2 \left(\overline{i_{in}^2} + \overline{i_1^2}\right) + \overline{i_2^2} + g_{ms2}^2 \overline{v_{ao}^2} \tag{2.9}$$

where $\overline{i_{in}^2}$, $\overline{i_1^2}$ and $\overline{i_2^2}$ are the mean square values of the input current noise and the current noise of M_1 and M_2 respectively. $\overline{v_{ao}^2}$ is the mean square value of the op-amp noise voltage referred to its input. Finally, g_{ms2} is the source transconductance of M_2.

2.3.3 FIRST GENERATION INTEGRATOR

The low-voltage SI technique proposed in [21] introduced the first generation SI integrator using the sample-hold circuit shown in Fig. 2.5. (b). The first generation SI lossy integrator is depicted in Fig. 2.6. (a). The timing clock diagram is illustrated in Fig. 2.6.(b).

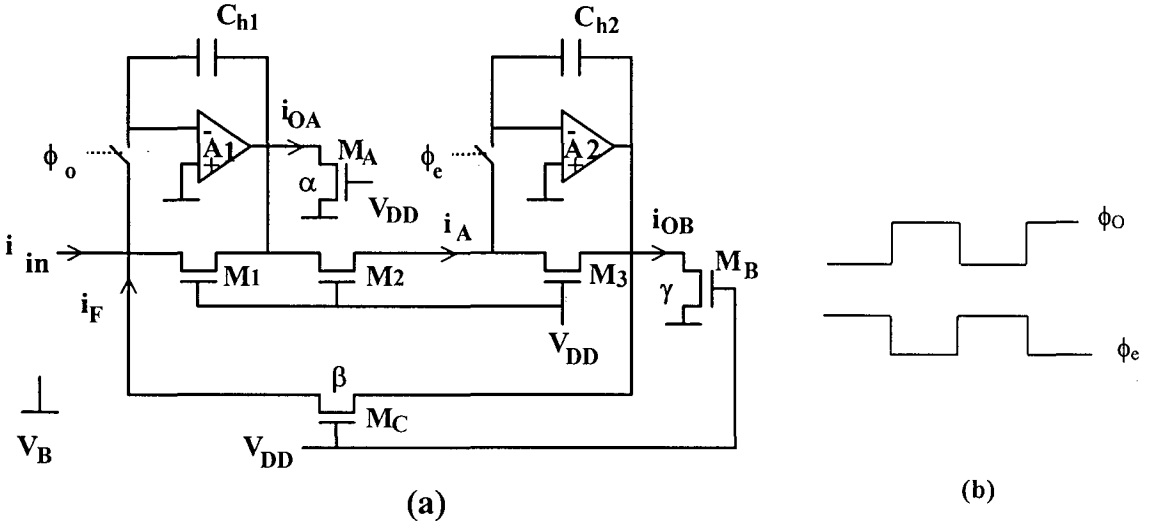


Fig. 2.6. First generation SI integrator for low-voltage applications.

(a) Circuit schematic.

(b) Clock sequence.

The integrator works as follows:

- During ϕ_o, the sum of the input and feedback currents is written in the first memory cell as a voltage across C_{h1};
- During ϕ_e, the input (i_A) to the second cell is stored as a voltage signal across C_{h2}.

Assuming M_1, M_2 and M_3 to be matched and to have the same aspect ratios, the integrator presents the following transfer functions at its outputs

$$\frac{I_{0A}^{\phi_o}(z)}{I_{IN}^{\phi_o}(z)} = -\alpha \frac{1}{1-\beta z^{-1}} \qquad (2.10.a)$$

$$\frac{I_{0B}^{\phi_o}(z)}{I_{IN}^{\phi_o}(z)} = \gamma \frac{z^{-1}}{1-\beta z^{-1}} \qquad (2.10.b)$$

Where $\alpha=(W/L)_{MA}/(W/L)_{M1}$, $\beta=(W/L)_{MC}/(W/L)_{M3}$ and $\gamma=(W/L)_{MB}/(W/L)_{M3}$.

2.4 THE CURRENT DIVISION TECHNIQUE AND THE MOCD STRUCTUTRE

The MOSFET-only current division technique was reported in [33]. In this work, the programmability of the SI filters is achieved through the MOSFET-only current dividers (MOCD's). The general schematic of the MOCD and its symbol [21, 33] are illustrated in Fig. 2.7. All transistors of the MOCD are connected to V_{SS} through a common substrate and have equal (W/L) aspect ratios. Therefore, the circuit operates as a binary current divider. Each binary fraction of the input current is injected into the SUM or DUMP lines according to the following rule:

$$b_i \begin{cases} 1 & \text{Current flows to SUM terminal.} \\ 0 & \text{Current flows to DUMP terminal.} \end{cases}$$

i = 1,2,3,.....M, and M is the MOCD resolution.

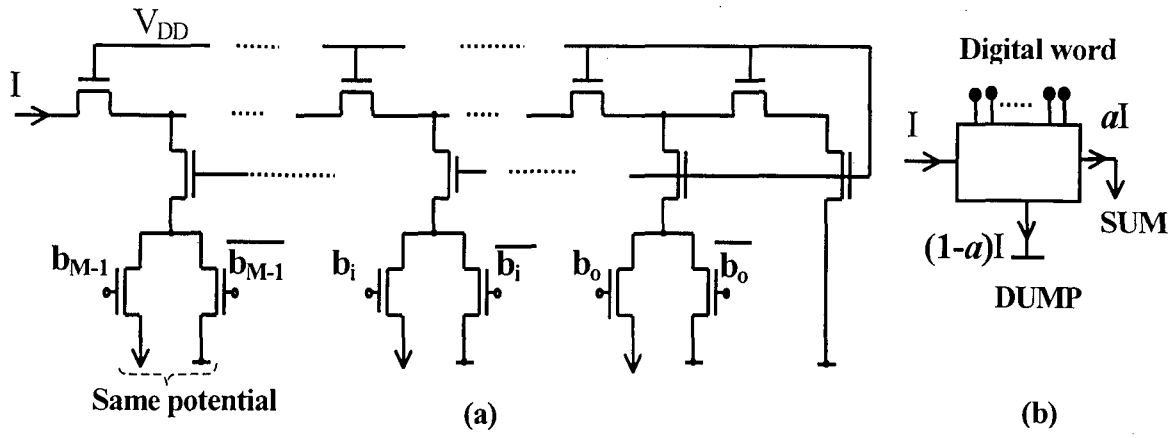


Fig. 2.7. The MOCD circuit scheme and its symbol.

The output current of the MOCD is a digitally controlled fraction (a) of the input current. This fraction is related to the digital control word as

$$a = \sum_{i=0}^{M-1} b_i 2^{(i-M)} \qquad (2.11)$$

Here, we use the MOCD as a digitally programmable coefficient with capability to implement the sign-bit. The MOCD has an input impedance which is independent of both the digital word and the number of bits, thus providing a constant load impedance to the op amps.

Several non-ideality parameters such as mobility degradation due to vertical field, velocity saturation, mismatch and noise produce errors. Analysis of these error sources and their influence on the performance of the MOCD is reported in [34]. The high linearity of the MOSFET-only current division technique has been proved adequate for analog signal processing [33, 34, 35].

- **AC ANALYSIS**

As regards DC analysis, the MOCD is equivalent to one transistor whose aspect ratio is one half the aspect ratio of a single transistor of the MOCD. For transient analysis,

the MOCD is equivalent to a nonlinear RC network. The exact AC analysis of the MOCD is relatively complicated. In a digital to analog (D/A) converter [35], only the parasitic capacitor associated with M_3 and M_4 in Fig. 2.8 has been considered for transient analysis. In other words, the MOCD time constant is the necessary time for the current to be deviated from one branch to the other (DUMP and SUM).

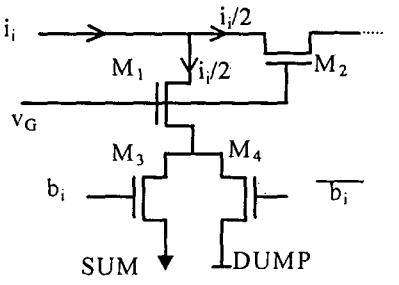


Fig. 2.8. The i^{th} bit of the MOCD in Fig. 2.7.

In this work, we will approximate each one-bit section as one transistor. From the MOST model [22], the intrinsic cutoff frequency of an MOS transistor can be approximated as:

$$f_T = \frac{\mu\phi_t}{2\pi L^2} 2\left(\sqrt{1+i_f} - 1\right) \tag{2.12}$$

Details about MOS transistor modeling are presented in Appendix A.

An M-bit MOCD can be considered as the cascade of M sections, where each section is equivalent to a single transistor. For worst case analysis, we will assume that the bits are settled in cascade. The total delay time can be approximated as

$$\tau_{Total} = \sum_{i=1}^{M} \tau_{ui} \cong M\,\tau_u \tag{2.13}$$

where τ_{ui} is the delay of the i^{th} section and all sections are assumed to have equal delays.

The intrinsic cutoff frequency for the MOCD can be approximated as $(1/2\pi\tau_{Total.})$. Thus, the maximum MOST channel length (L) that can be used is

$$L \le \sqrt{\frac{\mu.\phi_t}{M.2\pi.f_T} 2\left(\sqrt{1+i_f}-1\right)} \qquad (2.14)$$

The MOSFET maximum channel length can be approximated using (2.14), assuming $f_T=10F_{CK}$.

To verify our analysis, a 6-bit MOCD for 20 MHz clock frequency has been designed and simulated with 40μA (1 MHz) input current. The time and frequency responses are illustrated in Fig.2.9. The frequency response shows that the cutoff frequency is approximately 180 MHz, which is satisfactory for our application (10 MHz cutoff frequency).

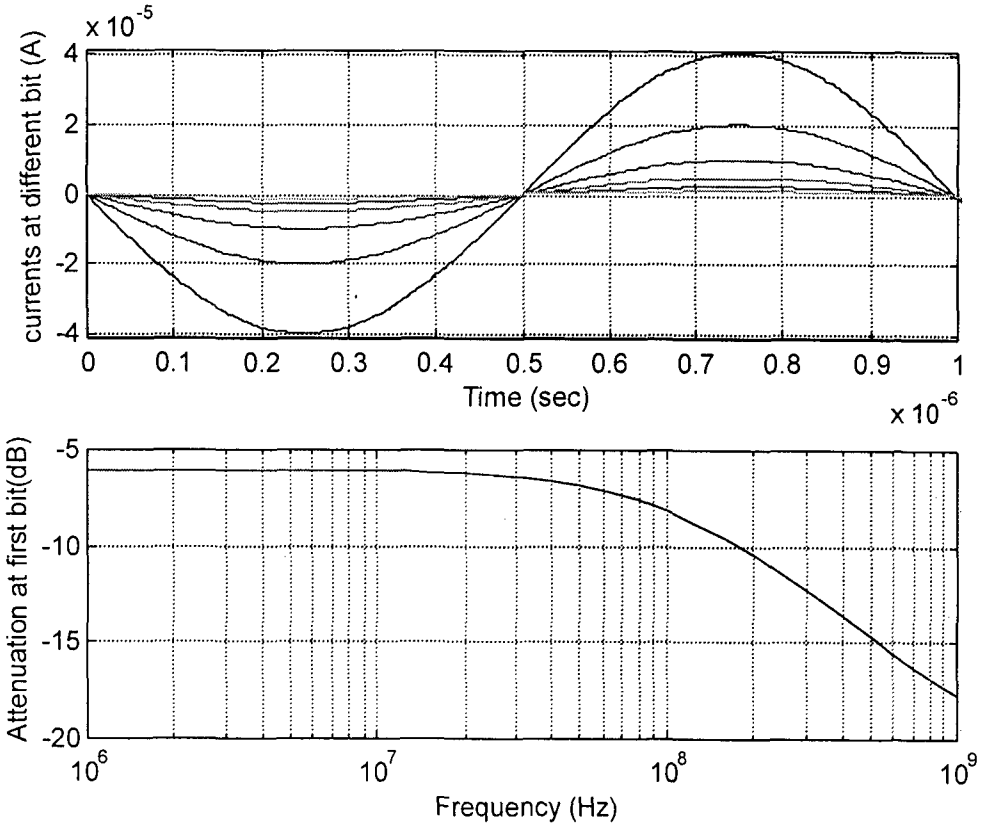


Fig. 2.9. The time and frequency response of the MOCD in Fig. 2.7.

CHAPTER 3

PROGRAMMABLE SECOND GENERATION SWITCHED-CURRENT INTEGRATOR AND BIQUAD FOR LOW-VOLTAGE APPLICATIONS

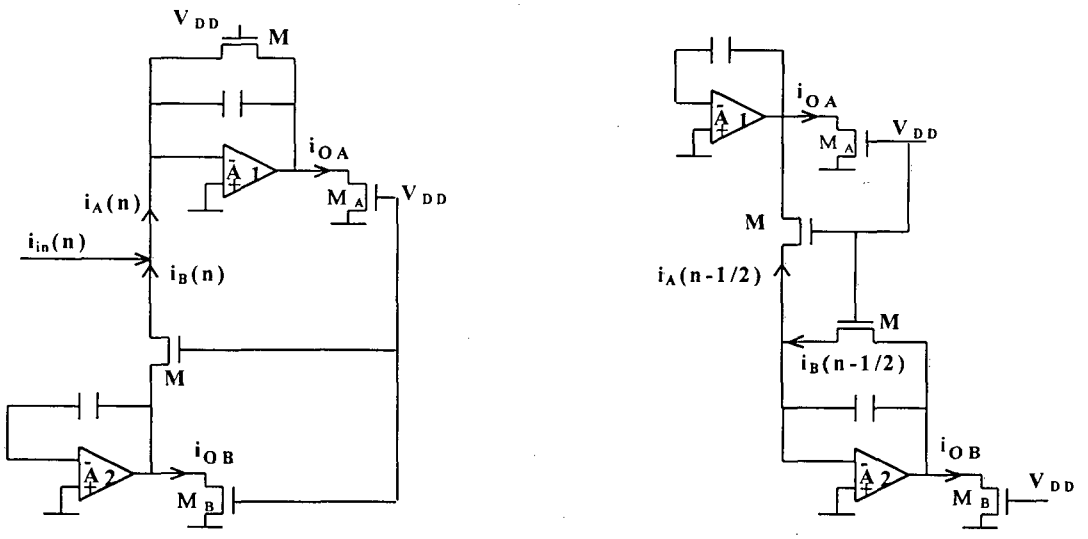
3.1 INTRODUCTION

In this chapter we propose a second generation SI integrator. The proposed integrator has been prototyped and programmed by using MOSFET-Only Current Dividers (MOCD) [33]. The consequence of the op-amp offset on the integrator performance has been studied. A programmable integrator-based biquad, which allows independent tuning of the center frequency and the quality factor has been implemented.

3.2 SECOND GENERATION INTEGRATOR

3.2.1 BASIC CELL

In this section, we propose a second generation SI integrator based on the SI mirror proposed in [21]. The proposed integrator is made up of two switched-current memory cells. Fig. 3.1 shows the proposed integrator at different clock phases. Two outputs are available, i_{OA} and i_{OB}. As in the conventional second generation SI integrator (Fig. 2.4. (b)), the input current together with the feedback current are fed to the first S/H (M_1) at the first half cycle. At the next half clock cycle, the stored signal is held on the second S/H (M_2).



(a) At t=n. **(b)** At t = n-1/2.

Fig. 3.1. The low-voltage SI integrator on different phases.

The analysis of the integrator at the two clock phases is as follows:

$$i_{OA}(n) = -\alpha\, i_A(n) = -\alpha\{i_{in}(n) + i_B(n)\} \tag{3.1.a}$$

and

$$i_B(n) = i_B(n-1/2) \tag{3.1.b}$$

On the previous half cycle, the currents are

$$i_B(n-1/2) = i_A(n-1/2) \tag{3.1.c}$$

and

$$i_A(n-1/2) = i_A(n-1) \tag{3.1.d}$$

From (3.1), we can write

$$i_{OA}(n) = -\alpha\, i_{in}(n) + i_{OA}(n-1) \tag{3.2.a}$$

and

$$i_{OB}(n) = \gamma\, i_{in}(n-1) + i_{OB}(n-1) \tag{3.2.b}$$

where $\alpha = (W/L)_{MA}/(W/L)_M$ and $\gamma = (W/L)_{MB}/(W/L)_M$. W and L are the channel width and length, respectively.

The z-transform of (3.2.a) and (3.2.b) gives:

$$\frac{I_{OA}^{\phi_o}}{I_{in}^{\phi_o}} = -\alpha \frac{1}{1-z^{-1}} \tag{3.3.a}$$

$$\frac{I_{OB}^{\phi_o}}{I_{in}^{\phi_o}} = \gamma \frac{z^{-1}}{1-z^{-1}} \tag{3.3.b}$$

An SI integrator which allows for the possibility of several input currents together with its timing diagram are illustrated in Fig 3.2. This timing diagram is necessary to avoid the loss of information during clock transition in a practical implementation.

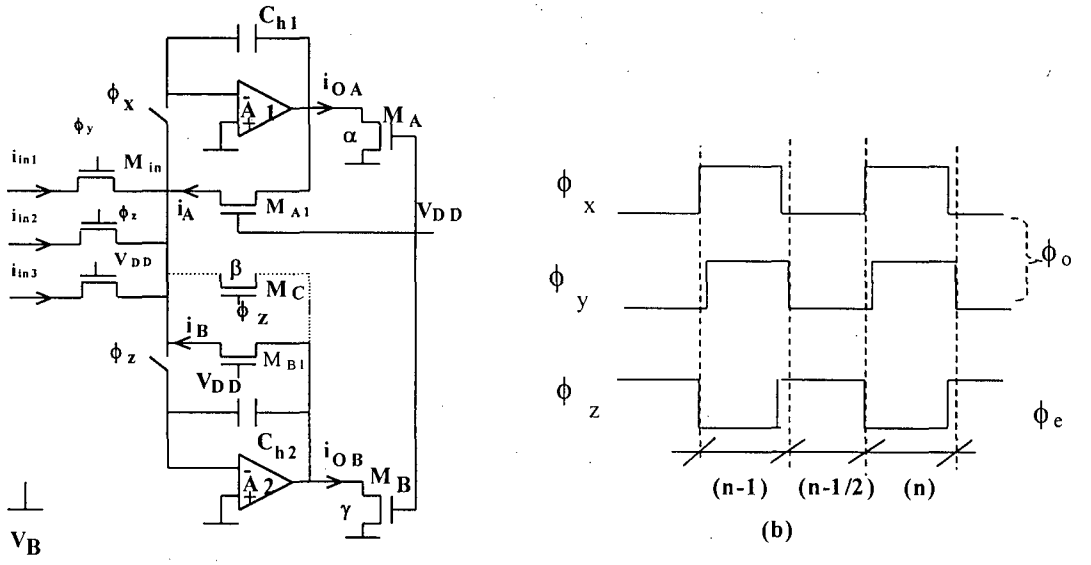


Fig. 3.2. The low-voltage second generation SI integrator.

(a) Circuit schematic.

(b) Clock phases.

Assuming that all MOS transistors have the same aspect ratios (W/L), the output/input relations are summarized in Table. 3.1. The continuous input (i_{in3}) is a sampled/held signal. If i_{in3} is sampled on the odd phase and held on the even phase, it is denoted as (odd+even). Conversely, if it is sampled on the even phase and held on the odd phase it is denoted as (even+odd). Table 3.1 illustrates that the proposed integrator allows performing forward, backward, and lossless discrete integrators which together, with inversion, give some flexibility for the biquad design.

Table 3-1. Transfer functions of the SI integrator in Fig. 3.2 (a).

	$I_{in1}^{\phi_o}$	$I_{in2}^{\phi_e}$	Continuous signal (I_{in3})	
			odd+even[1]	Even+odd[2]
$I_{OA}^{\phi_o}$	$-1 / (1-z^{-1})$	$z^{-1/2} / (1-z^{-1})$	-1	0
$I_{OA}^{\phi_e}$	$-z^{-1/2} / (1-z^{-1})$	$z^{-1} / (1-z^{-1})$	$-z^{-1/2}$	0
$I_{OB}^{\phi_o}$	$z^{-1} / (1-z^{-1})$	$-z^{-1/2} / (1-z^{-1})$	0	$-z^{-1/2}$
$I_{OB}^{\phi_e}$	$z^{-1/2} / (1-z^{-1})$	$-1 / (1-z^{-1})$	0	-1

1. An odd+even signal is sampled at ϕ_o and held constant at ϕ_e.
2. An even+odd signal is sampled at ϕ_e and held constant at ϕ_o.

A lossy SI integrator can be realized using the dotted feedback path shown in Fig. 3.2. (a). The z-domain transfer functions are:

$$\frac{I_{OA}^{\phi_o}}{I_{in}^{\phi_o}} = -\alpha \frac{1}{1+\beta-z^{-1}} \tag{3.4.a}$$

$$\frac{I_{OB}^{\phi_o}}{I_{in}^{\phi_o}} = \gamma \frac{z^{-1}}{1+\beta-z^{-1}} \tag{3.4.b}$$

where $\beta=(W/L)_{MC} / (W/L)_{MB1}$ and $i_{in}=i_{in1}$.

The MOS transistor responsible for the loss must be clocked in the even phase; otherwise, the feedback factor would be $(1+\beta)I_{OB}z^{-1}$ which means that the integrator would become unstable.

The integrator with this topology has an axis that divides it into two identical sections, thus reducing the effects of charge injection [25]. Ideally, the charges injected by the two switches and clock feedthrough are equal. However, current errors due to charge injection are not canceled out due to circuit mismatch and nonlinearities. The proposed second generation SI integrator has the same sensitivities to transistor

mismatch [32] as the conventional second generation SI integrator in [20]. In the integrator proposed here, the switches operate at constant voltage [36, 37], which means that the charge injected into the holding capacitors (C_{h1} and C_{h2}) is signal-independent. Thus, the proposed integrator is capable of achieving higher accuracy than the conventional SI integrator. Moreover, if the voltage V_x obtained from the network in Fig. 2.5.(c) is applied into the non-inverting input of the op-amps, the conduction gap [8, 10] existing in conventional SI circuits is avoided. Therefore, the SI topologies proposed here are more suitable for low voltage applications than the conventional ones.

- **SIMULATION**

The SI integrator shown in Fig. 3.2.(a) has been simulated using the SMASH [38] simulator together with ACM MOSFET model [22]. The circuit was simulated for 8μA (20kHz) input signal, 1MHz sampling rate and C_{h1}= C_{h2}=0.5pF. The aspect ratios are 5.6μm/5.6μm for the MOS transistor and 3μm/0.7μm for the nMOS switches. The detailed design of the two-stage op-amp is presented in Appendix B. The simulation result is shown in Fig. 3.3. The offset between i_{AO} and i_{OB} is due to the offset voltage mismatch between the opamps. A linear voltage-to-current converter has been implemented using a linear resistor.

3.2.2 THE EFFECT OF THE OP-AMP OFFSET VOLTAGE

Fig. 3.4 illustrates the proposed SI integrator considering op-amp offsets. The operating voltages of the switches are V_B+V_{OFF1} or V_B+V_{OFF2}. This difference generates a current error proportional to the difference between the offsets. This problem is

exactly the same as in the conventional SI integrator if mismatch between the current sources (see Fig. 2.4) is taken into account.

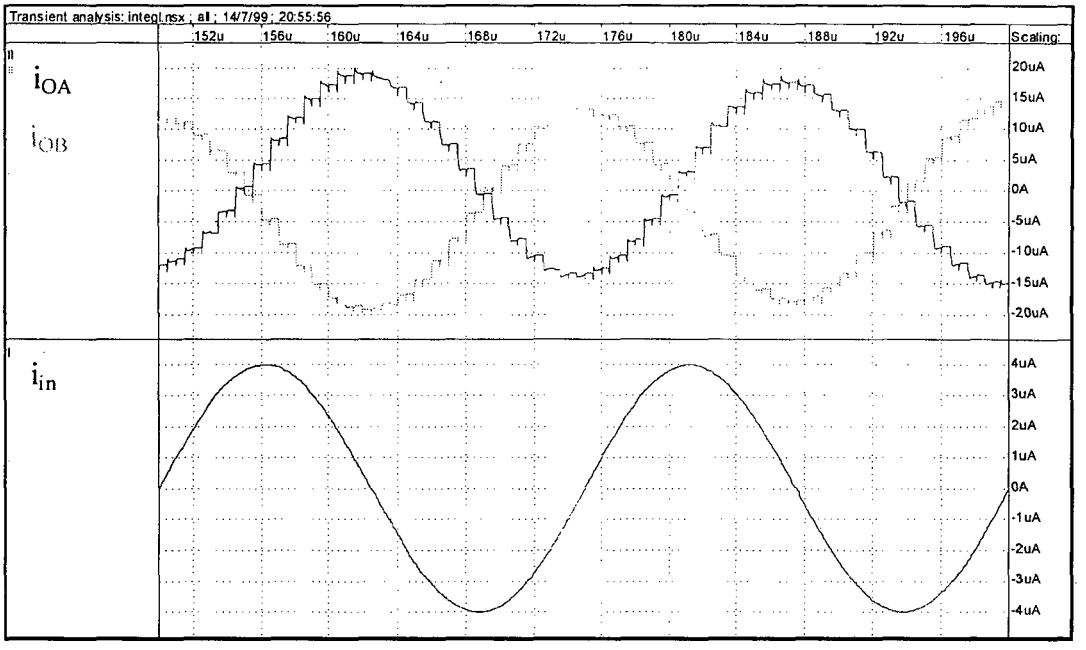


Fig. 3.3. Sinusoidal steady state response of the low-voltage integrator.

In this section, we analyze the effects of the op-amp offsets on the output voltage. The offset voltages have been considered as time-invariant signals and the input current is zero. The analysis of the SI second generation integrator leads to:

$$V_{OA}^{o} = \frac{B' + A - Az^{-1}}{A(1-z^{-1})} V_{OFF1}^{o} + \frac{z^{-1/2}}{1-z^{-1}} V_{OFF1}^{e} - \frac{B}{A(1-z^{-1})} V_{OFF2}^{o} - \frac{A'z^{-1/2}}{A(1-z^{-1})} V_{OFF2}^{e} \quad (3.5.a)$$

$$V_{OA}^{e} = \frac{B'z^{-1/2}}{A(1-z^{-1})} V_{OFF1}^{o} + \frac{1}{1-z^{-1}} V_{OFF1}^{e} - \frac{Bz^{-1/2}}{A(1-z^{-1})} V_{OFF2}^{o} - \frac{A'z^{-1}}{A(1-z^{-1})} V_{OFF2}^{e} \quad (3.5.b)$$

$$V_{OB}^{o} = -\frac{B'z^{-1}}{B(1-z^{-1})} V_{OFF1}^{o} - \frac{Az^{-1/2}}{B(1-z^{-1})} V_{OFF1}^{e} + \frac{1}{(1-z^{-1})} V_{OFF2}^{o} + \frac{A'z^{-1/2}}{B(1-z^{-1})} V_{OFF2}^{e} \quad (3.5.c)$$

$$V_{OB}^{e} = -\frac{B'z^{-1/2}}{B(1-z^{-1})} V_{OFF1}^{o} - \frac{A}{B(1-z^{-1})} V_{OFF1}^{e} + \frac{z^{-1/2}}{(1-z^{-1})} V_{OFF2}^{o} + \frac{A' + B - Bz^{-1}}{B(1-z^{-1})} V_{OFF2}^{e} \quad (3.5.d)$$

$A\alpha(W/L)_{MA1}$, $B\ \alpha\ (W/L)_{MB1}$, $A' = A + \sum K_{in}^{e}$, $B' = B + \sum K_{in}^{o}$ and $K^{o}_{in}\ \alpha\ (W/L)_{Min}$

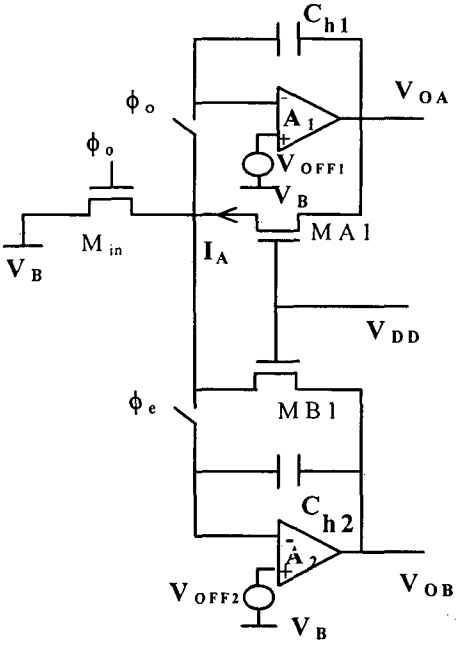


Fig. 3.4. Scheme of the low-voltage SI integrator including op-amp offset voltages.

The error in the output current I_A at odd phase is denoted by ΔI_A^{o}

$$\Delta I_A^{O}(Z) = A\left[(V_{OA}^{O} - V_{OFF1}^{O}) - Z^{-1/2}(V_{OA}^{e} - V_{OFF2}^{e})\right] \tag{3.6}$$

Assuming zero initial condition and zero input (no current at M_{in} due to offset voltages), the output current (I_A) due to the offset voltages is

$$I_A^{o}(1 - z^{-1}) = B(V_{OFF1}^{o} - V_{OFF2}^{o}) \tag{3.7}$$

Therefore, if the two op-amps have equal offset voltages, the current error will tend to zero. However, for the general case $V_{OFF1} \neq V_{OFF2}$, and the difference in the offset voltages will affect the dynamic range of the circuits. Thus, the op-amp offset presents a major problem for the proposed integrator. So it is important to overcome this drawback by using dynamic [39] or offset compensation techniques as in SC circuit [40].

- **OFFSET COMPENSATION [40]**

Fig. 3.5.(a) illustrates an SI sample-hold circuit with offset compensation. The circuit works as follows. When ϕ_c is high, the offset voltage is stored into C_c. Consequently, when ϕ_c is low the offset appears as an input signal and its effects are ideally canceled out.

The switches in Fig. 3.5.(a) still work at constant DC voltage. Thus, this circuit avoids the conduction gap. The offset-insensitive second generation SI integrator is shown in Fig. 3.5.(b).

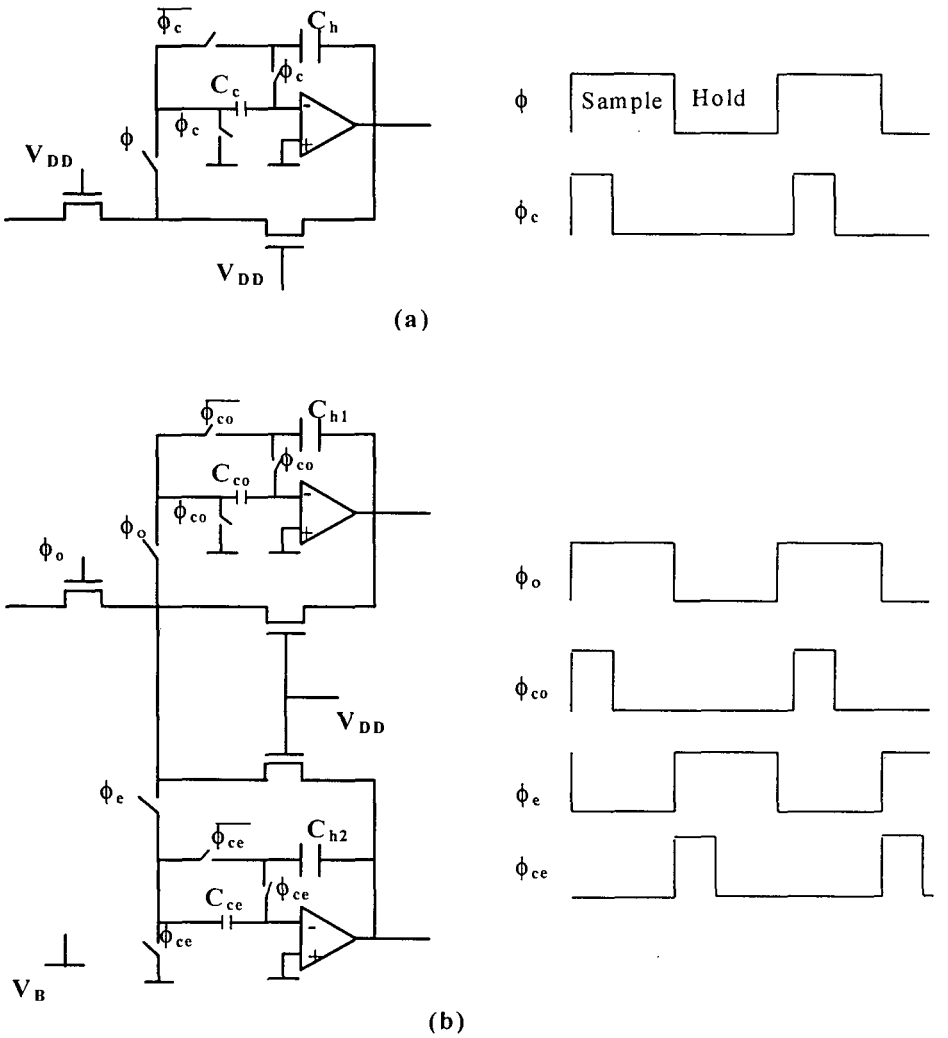


Fig. 3.5. Offset compensation for the SI technique [40].

(a) Sample hold circuit.

(b) Second generation integrator and clock diagram.

- **EXPERIMENTAL RESULTS** [1]

The SI lossy integrator shown in Fig. 3.2.(a) was implemented using operational amplifiers TL 082, MOS integrated transistors (W=48μm, L=1.2 μm), MOS switches CD 4007 and holding capacitors of 1.8nF. The loss factor (β) was set by a 6-bit MOSFET-Only Current Divider (MOCD). The 6-bit MOCD was integrated on a Sea-of-Transistors (SoT) array, in a 1.2μm technology from ES2 [41]. The MOCD is switched by "ANDing" the digital word and the even phase waveforms $\{\phi_e.\mathbf{b}(b_{N-1} \ldots\ldots b_o)\}$. The integrator has been simulated using the ASIZ program [42]. The simulated and experimental frequency responses presented in Fig. 3.6 show excellent agreement.

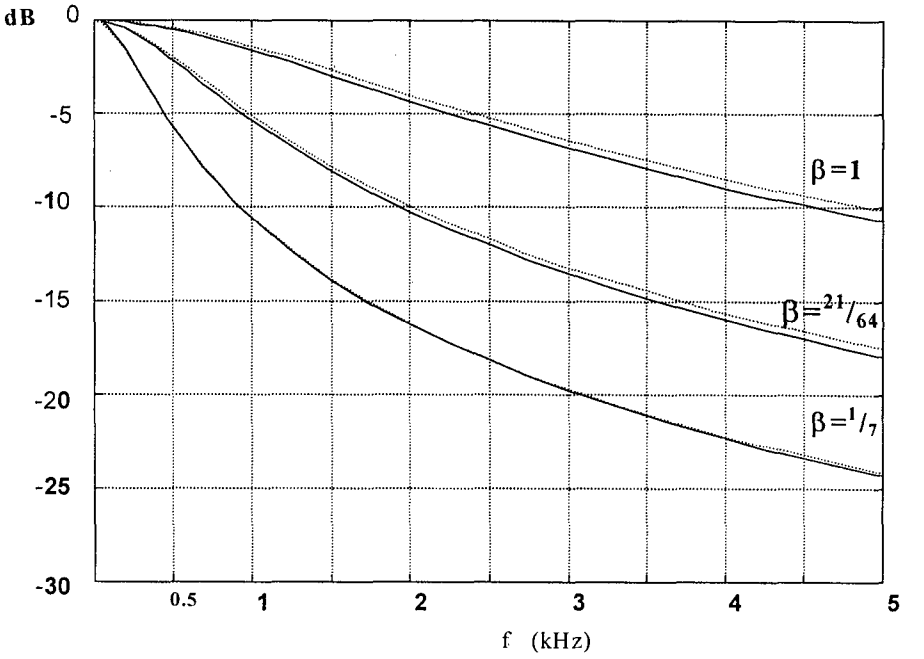


Fig. 3.6. Frequency response of the low-voltage second generation SI integrator in Fig.3.2 ..... -Theoretical and __-Experimental.

[1] The experimental work has been done by M. Sc. Renato Faustino.

3.3 SECOND ORDER SECTION

The second generation SI integrator has been applied to a programmable second order biquad. In this biquad section, the normalized center frequency (ω_O T) and the quality factor (Q) can be controlled independently. The design algorithm, the prewarped error and the switched current realization of the biquad section are described next.

3.3.1 GENERAL BLOCK DIAGRAM

The block diagram of a second order filter is shown in Fig. 3.7. The general transfer function is

$$\frac{X_{O/P}(S)}{X_{IN}(S)} = -\frac{K_3S^2 + K_2a_1fS + K_1a_1a_2}{S^2 + a_1fS + a_1a_2} \tag{3.8}$$

where S=sT is the normalized frequency.

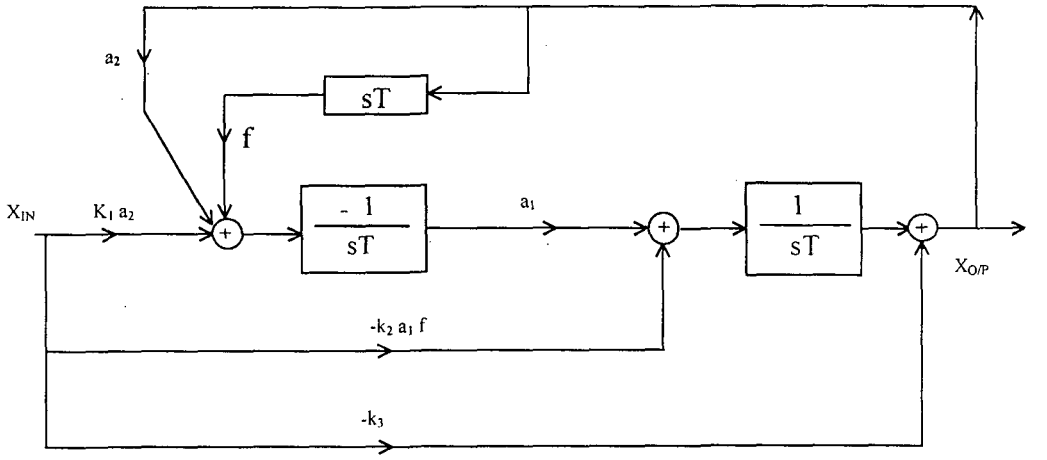


Fig. 3.7. Block diagram of a biquad.

In (3.8), the normalized center frequency and quality factor of the biquad are described as

$$\omega_o T = \sqrt{a_1 a_2} \tag{3.9.a}$$

$$Q = \frac{1}{f}\sqrt{\frac{a_2}{a_1}} \qquad (3.9.b)$$

where ω_o is center frequency and Q is the quality factor.

This biquad allows one to obtain low-pass (K_2 and K_3 = 0), bandpass (K_1 and K_3 = 0), high-pass (K_1 and K_2 =0), band-reject (K2=0), and all-pass filters.

3.3.2 MAPPING ERROR ANALYSIS

A common approach to design sampled-data filter is to obtain H (z) from the s-domain transfer function H (S). The mapping from the S- to the Z-domain is achieved via a transformation of the frequency variable. In this work, we will obtain the biquad circuit parameters directly from the analog specifications, namely, the center frequency (ω_O), the quality factor (Q) and the gain (K_o) at the center frequency. The errors in center frequency, quality factor and gain owing to frequency mapping must be taken into account. The error in both ω_O and Q due to prewarping have been studied elsewhere [43]. In this section, the magnitude error {|H (i ω_O)|} at the center frequency has been analyzed as follows.

The power series of the z-domain variable up to the second order term is

$$z^{-1} = e^{-i\omega T} \approx 1 + (-i\omega T) + (-i\omega T)^2/2! + (-i\omega T)^3/3! \qquad (3.10)$$

The application of backward Euler transformation ($ST=1-z^{-1}$) to the bandpass filter (K_1 and K_3 =0 in equation 3.8) leads to

$$H(z) = \frac{K_2 \frac{\omega_o T}{Q}(1-z^{-1})}{(1-z^{-1})^2 + \frac{\omega_o T}{Q}(1-z^{-1}) + (\omega_o T)^2} \qquad (3.11)$$

From (3.10) and (3.11), the magnitude of the transfer function at the center frequency $\{|H(i\omega_O T)|\}$ is

$$|H(i\omega_O T)| \approx \frac{K_2}{\omega_O TQ + 1} \tag{3.12}$$

which is equal to K_2 if $Q\omega_o T << 1$

Fig.3.8 shows the magnitude error at the center frequency as function of the normalized frequency (F_o/F_{CK}) for different quality factors. F_o is equal to $2\pi/\omega_o$ and F_{CK} is equal to 1/T. The error can be very large specially for high-Q filters and large F_o/F_{CK} ratios. The error of the backward LDI transformation [43] leads to a considerably smaller magnitude error at F_o, as shown in Fig. 3.9.

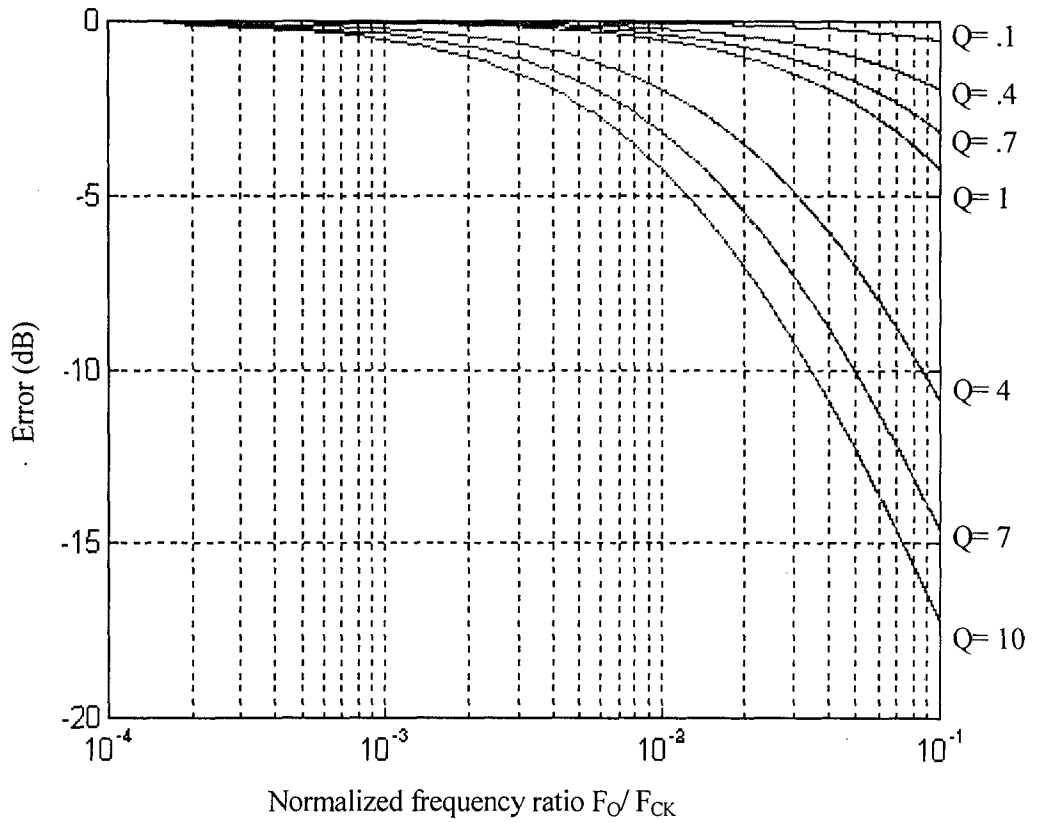


Fig. 3.8. Magnitude error at the center frequency for backward Euler transformation.

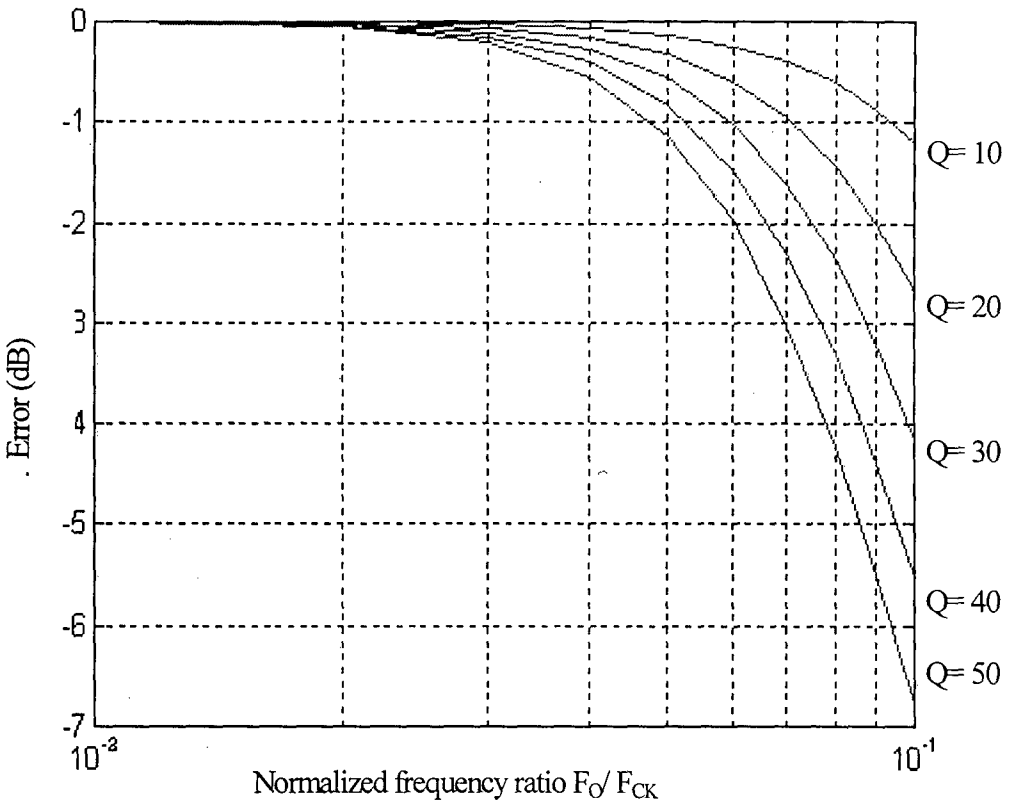


Fig. 3.9. Magnitude error at the center frequency for the backward LDI transformation.

3.3.3 IMPLEMENTATION OF THE SWITCHED-CURRENT BIQUAD

As an application of the proposed SI integrator, we have designed a biquadratic section by using backward LDI transformation [43]. The biquad presented in Fig. 3.7 has been realized as shown in Fig. 3.10. The output current as function of the inputs is

$$I_o(z) = -\frac{K_3.I_3.(1-z^{-1})^2 + K_2.I_2a_2.f.(1-z^{-1})z^{-1} + K_1.I_1.a^2z^{-1}}{1-(2-a_1.f-a_1a_2)z^{-1}+(1-a_1f).z^{-2}} \qquad (3.13)$$

Using $z \cong 1+sT+ (sT)^2/2!$ in (3.13), the normalized center frequency (ω_oT) and the quality factor (Q) can be approximated as

$$\omega_o T = \sqrt{\frac{a_1 a_2}{1 - a_1 f}} \qquad (3.14.a)$$

$$Q = \frac{\sqrt{(1 - a_1 f) a_1 a_2}}{a_1 - f} \qquad (3.14.b)$$

When $a=a_1=a_2$, $a << 1$ and $af<<1$, both $\omega_o T$ and Q are controlled independently if the sampling frequency is much higher than the center frequency. In this case:

$$\omega_o T \cong a \qquad \text{and} \qquad Q \cong 1/f$$

The programmability of the biquad is achieved using the MOCD device [33]. In Fig. 3.10, the term "ϕ.x" means that the digital word "x" is ANDing with clock "ϕ" to implement the switching of the MOCD.

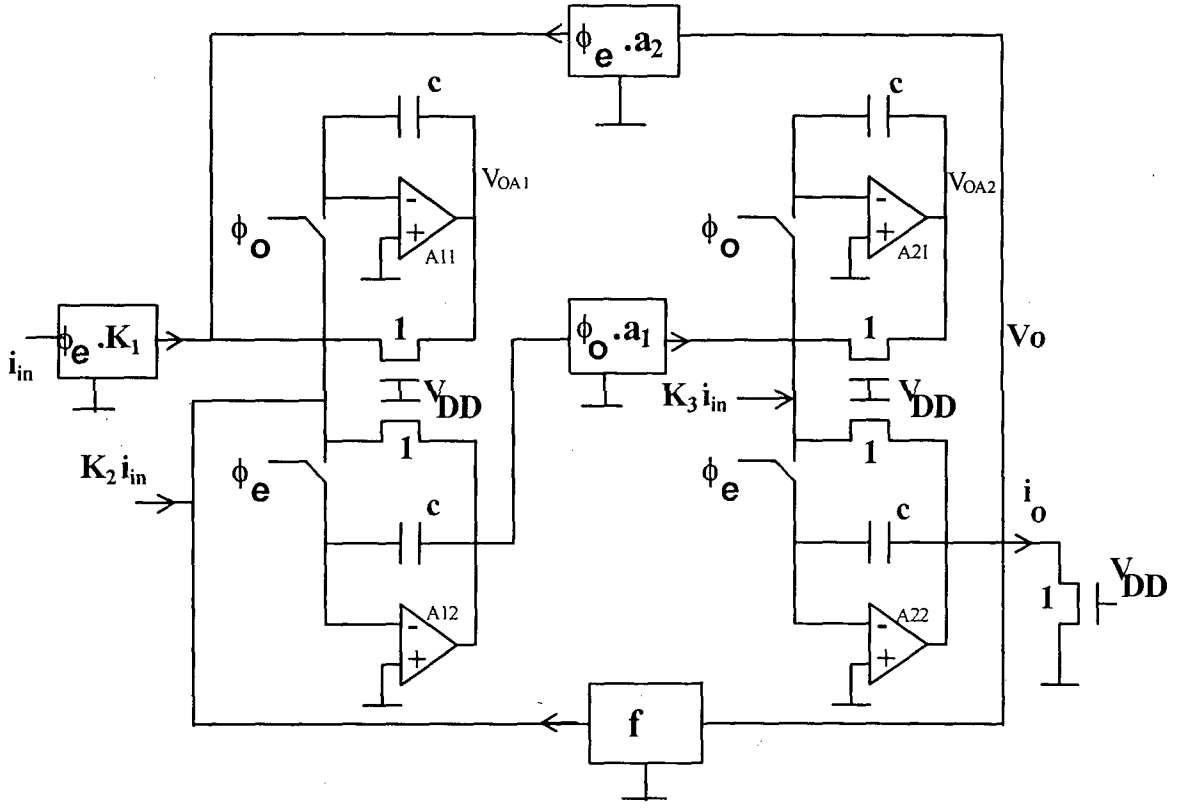


Fig. 3.10. Biquadratic section using second-generation SI integrators.

- **EXPERIMENTAL RESULTS**[1]

A discrete prototype of the filter has been implemented and tested. In this experimental work, transistors were replaced by resistors. The programmability of the filter was obtained by scaling the resistances. The unit resistor is 20kΩ, and the holding capacitors are C=100pF. The bandpass filter has been programmed for center frequencies f_o=150, 300 and 600Hz. The sampling frequency was 15kHz and the quality factor was equal to 8. The simulation and experimental results are shown in Fig. 3.11. In the case of very low $\omega_o T$, the error in the center frequency is large due to the variability of the resistors. To reduce this error we have to decrease the variability of the resistance or, for an IC implementation, increase the resolution of the MOCD.

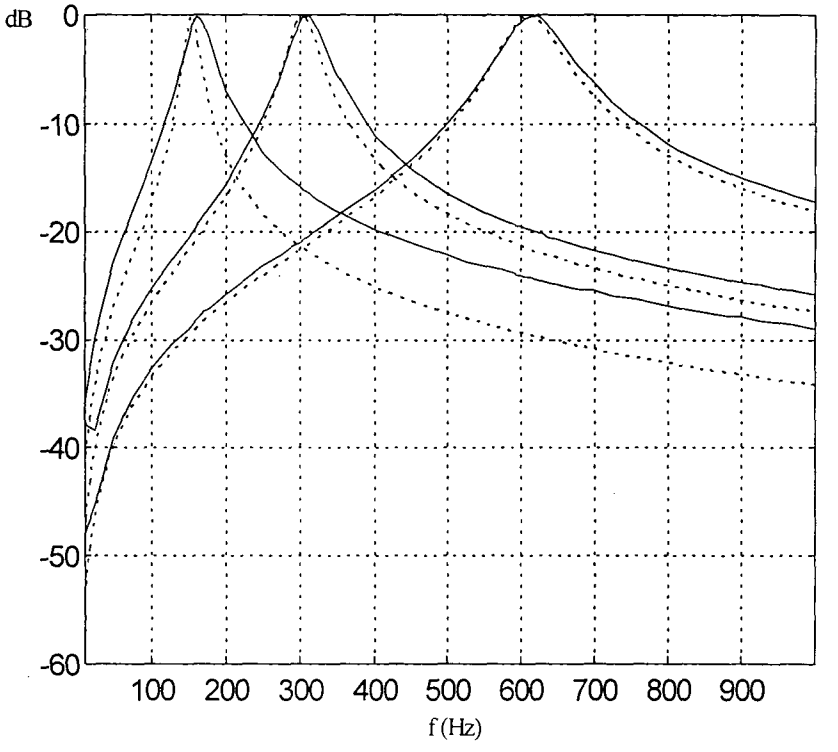


Fig. 3.11. Theoretical (....) and experimental (___) magnitude response of the bandpass filter. f_o=150, 300 and 600 Hz (Q=8 and F_{CK}=15kHz).

[1] The experimental work has been done by the M. Sc. Renato Faustino.

3.3.4 EFFECT OF THE OFFSET VOLTAGE OF THE OP-AMPS ON THE BIQUAD OUTPUT

As we have seen, the proposed SI integrator suffers from mismatch between the op-amp offset voltages. The output voltages due to op-amp offsets are:

$$V_{OA2}^{o}\{(1-z^{-1})^2+a_1a_2z^{-1}+a_1fz^{-1}(1-z^{-1})\}=$$
$$\begin{aligned}&(2+k_3)\ (1-z^{-1})\ V_{12}\\&-(1+(1+a_1+k_2+k_3)z^{-1})(1-z^{-1})\ V_{22}\\&+a_1z^{-1}(k_1+a_2+f+2)\ V_{11}\\&-a_1z^{-1}(1+(1+f)z^{-1})\,V_{21}\end{aligned}\qquad (3.15.a)$$

$$V_{OA1}^{e}\{(1-z^{-1})^2+a_1a_2z^{-1}+a_1fz^{-1}(1-z^{-1})\}=$$
$$\begin{aligned}&+\{1+(k_1+a_2+f+1)z^{-1}\}(1-z^{-1})\,V_{11}\\&-(2+f)z^{-1}(1-z^{-1})V_{21}\\&(2+k_3)\{a_2+f(1-z^{-1})\}V_{12}\\&-(1+(1+a_1+k_2+k_3)z^{-1})\quad(a_2+f(1-z^{-1})\,V_{22}\end{aligned}\qquad (3.15.b)$$

where V_{ij} is offset voltage of op-amp A_{ij} in Fig. (3.10), with i=1,2 and j=1,2.

To simplify expressions (3.15), we assume the offset to be a DC signal (z=1). Thus (3.15.a) and (3.15.b) become

$$V_{OA2}^{o}=\frac{k_1+a_2+f+2}{a_2}V_{11}-\frac{2+f}{a_2}V_{21}\qquad a_2=\omega_oT\langle\langle\quad 1 \qquad (3.16.a)$$

$$V_{OA1}^{e}=\frac{k_3+2}{a_1}V_{12}-\frac{2+K_2+K_3+a_1}{a_1}V_{22}\qquad a_1=\omega_oT\langle\langle\quad 1 \qquad (3.16.b)$$

where $K_1/a_2 = G_{DC}$ (DC gain), $f/a_2 = 1/(Q\ \omega_oT)$, $K_2/a_1 = Q\ G\ (\omega_oT)$ and $K_3/a_1 = G_{HF}/\omega_oT$.

Finally, the DC output caused by the op-amp offsets, Eqn. (3.16.a), is written as

$$V_O=(1+G_{DC})V_{off1}+(2+\frac{1}{Q})\frac{\Delta V}{\omega_oT} \qquad (3.17)$$

where ΔV is the offset mismatch $\{V_{off1}(A_{11})-V_{off2}(A_{12})\}$.

The DC component of the output, as given by (3.17), is not large provided that the sampling frequency is not very much higher than the center frequency of the biquad or the offset mismatch is not high. The dynamic technique presented in section (3.2.2) can be employed to reduce the effects of the offset mismatch.

CHAPTER 4

PROGRAMMABLE SWITCHED-CURRENT SAMPLE-HOLD CIRCUITS

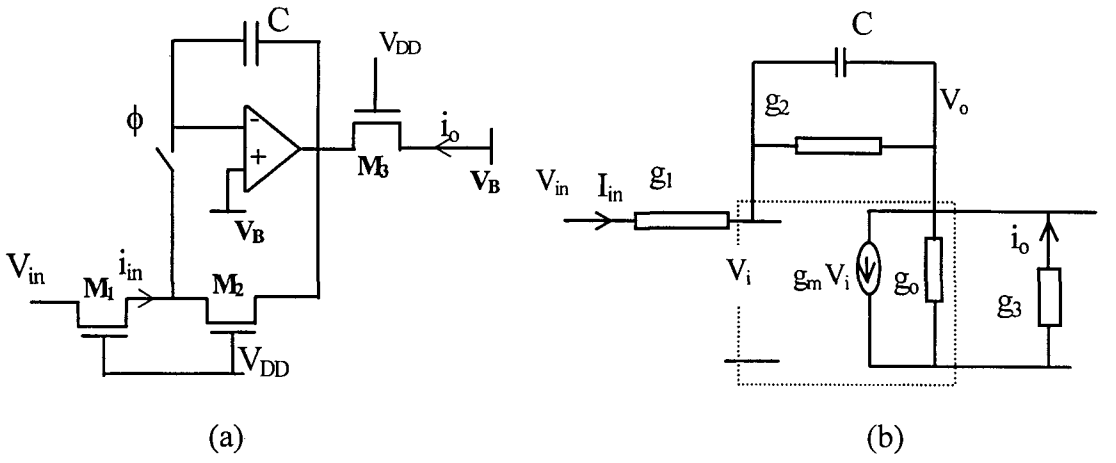
4.1 INTRODUCTION

Field programmable integrated circuits (ICs) are receiving increased attention. Particularly, programmable filters can be used in signal processing applications such as adaptive filters, spectral analysis, equalization, waveform synthesis and many others. CMOS programmable filters are typically implemented by using charge coupled devices (CCD) and switched-capacitor techniques. In the SC technique, digitally controlled binary-weighted C-arrays [44] or charge-programmability [45] are used to digitally program a filter. The C-array technique requires large silicon area compared with the SI technique while the charge programmability approach is slow. The most common methodologies to design programmable SI filters employ either digitally programmable conventional current mirrors [46, 47] or digitally controlled MOSFET-only attenuators [33]. Both approaches take advantage of the reduced area required to implement programmable current mode filters.

This chapter is dedicated to the analysis and design of programmable single-ended and fully balanced SI sample-hold circuits using the SI methodology of [21]. The programmability is achieved via the current division technique. The complete programmable S/H circuit has been designed for 20 MHz sampling rate.

4.2 SINGLE-ENDED SAMPLE-HOLD

In this section, the design of a switched-current S/H circuit for low-voltage applications is presented. The main objectives are to obtain the op-amp specification, the holding capacitor value and the MOS transistor aspect ratios. Fig. 4.1.(a) shows the circuit of the S/H.



(a) (b)

Fig. 4.1. The switched-current sampled-hold circuit.

(a) Scheme.

(b) Small-signal equivalent circuit.

In the small signal equivalent circuit illustrated in Fig.4.1.(b), the op-amp is assumed to have infinite bandwidth and the switch to be ideal. The transfer function H(s) of the S/H can be written as:

$$H(s) = \frac{G_o}{1+s\tau} \tag{4.1}$$

where

$$G_O = -\frac{g_1}{g_2}\frac{1-g_2/g_m}{1+\dfrac{g_1+g_L+g_Lg_1/g_2}{g_m}} \tag{4.2.a}$$

and

$$\tau = \frac{C}{g_2} \frac{1}{1 + \frac{g_L g_1 / g_2}{g_m + g_L + g_1}} \tag{4.2.b}$$

$g_L=g_3+g_o$ and g_1, g_2 and g_3 are the drain-source conductances of the MOSFETs, which in strong inversion are given by:

$$g_{mS} = \mu n C'_{ox} \frac{W}{L} (V_P - V_s) \tag{4.3}$$

The circuit in Fig. 4.1.(a) performs as an ideal inverting amplifier ($G_O \cong -g_1/g_2$) when

$$g_m >> g_1 + g_L + g_L g_1 / g_2 \tag{4.4.a}$$

In this case

$$\tau \approx \frac{C}{g_2} \tag{4.4.b}$$

Moreover, in high-speed applications, the settling error is an important issue. Using (4.1) at the end of the sampling phase (t = T/N) (N is the number of phases) the settling error is given by

$$\gamma = e^{(-T/N\,\tau)} \tag{4.5}$$

which affects the sample-hold transfer function [48] according to

$$H(z) = \frac{(1-\gamma)}{1-\gamma z^{-1}} z^{-1/2} \tag{4.6}$$

Moreover, the maximum value of the holding capacitance (C) such that the settling error is less than γ, can be expressed as

$$C < T g_2 / \{N \ln(1/|\gamma|)\} \tag{4.7}$$

However, C should be large enough to reduce the (kT/C) noise.

- **DESIGN STEPS**

As a conclusion about the previous analysis, the design steps are:

- The MOSFET maximum channel length can be approximated using (2.14), assuming $f_T=10F_{CK}$.
- (4.7) is used to obtain the required holding capacitor and channel width for a certain settling error.
- The total op-amp transconductance required can be approximated using (4.4.a) and the op-amp gain bandwidth product is selected as 10 g_2/ C.

- **PROGRAMMABLE S/H CIRCUIT**

This section is dedicated to the design of a programmable switched-current S/H circuit for 20MHz sampling rate applications. The programmability has been implemented using the MOCD structure. The programmable S/H circuit is depicted in Fig. 4.2. The circuit is designed for 1% settling error and 10MHz cutoff frequency. The design parameters are given in Table 4.1.

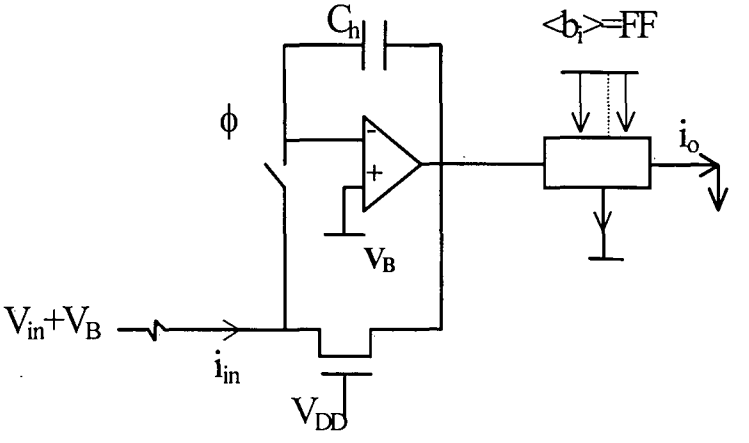


Fig. 4.2. Digitally programmable sampled-hold.

Table 4.1. Parameters of the sample-hold circuit.

(W/L) of any transistor of the MOCD	6μm/2.5μm	
Holding capacitor	0.5pF	$\sqrt{\frac{kT}{C}} \cong 91\mu V$.
(W/L) of nMOST switch	3μm/0.8μm	
Op-amp bandwidth	100MHz	
G_m(OTA)	55mA/V	Open loop gain >40dB

- **VERIFICATION**

To verify our design, the S/H circuit shown in Fig. 4.2 has been simulated using T-Spice [49]. The step and sinusoidal responses are shown in Fig. 4.3 and Fig. 4.4, respectively. Fig.4.3 shows that the output settles within 1% after 24ns from clock transition. In Fig. 4.4, the input noise is due to switch ϕ in Fig. 4.2. In Figs 4.3 and 4.4, the inputs are the current response of step and sinusoidal input voltages, respectively. Fig. 4.3 is simulated with typical MOSFET parameter. To study the effect of MOSFET parameter variation, the circuit must be simulated with fast and slow MOSFET parameter.

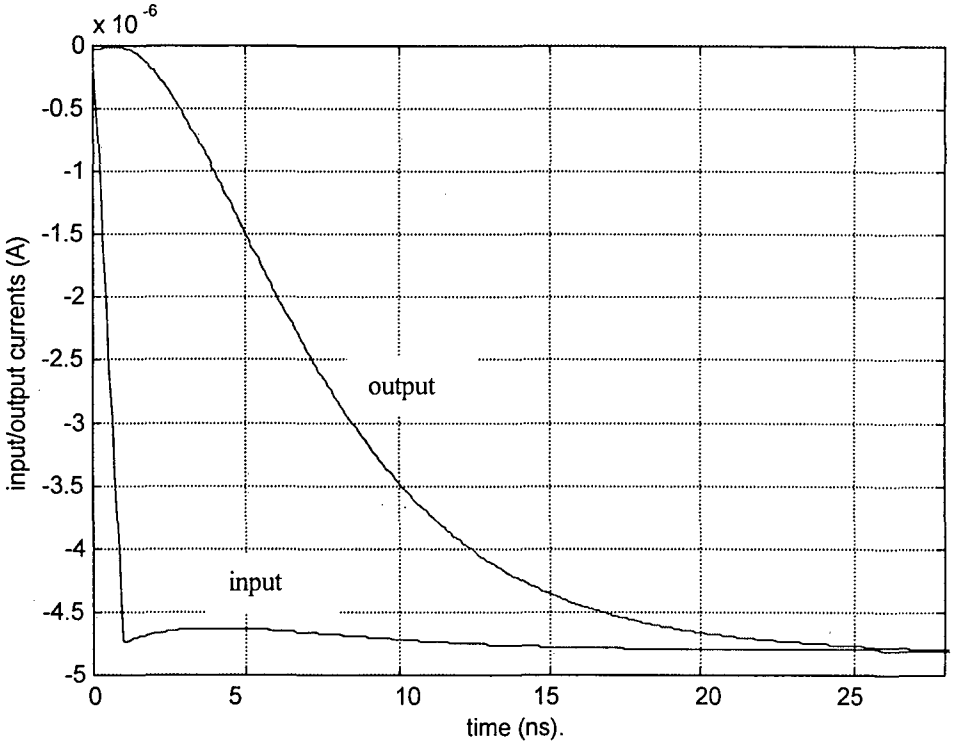


Fig. 4.3. The step response of the sample-hold circuit.

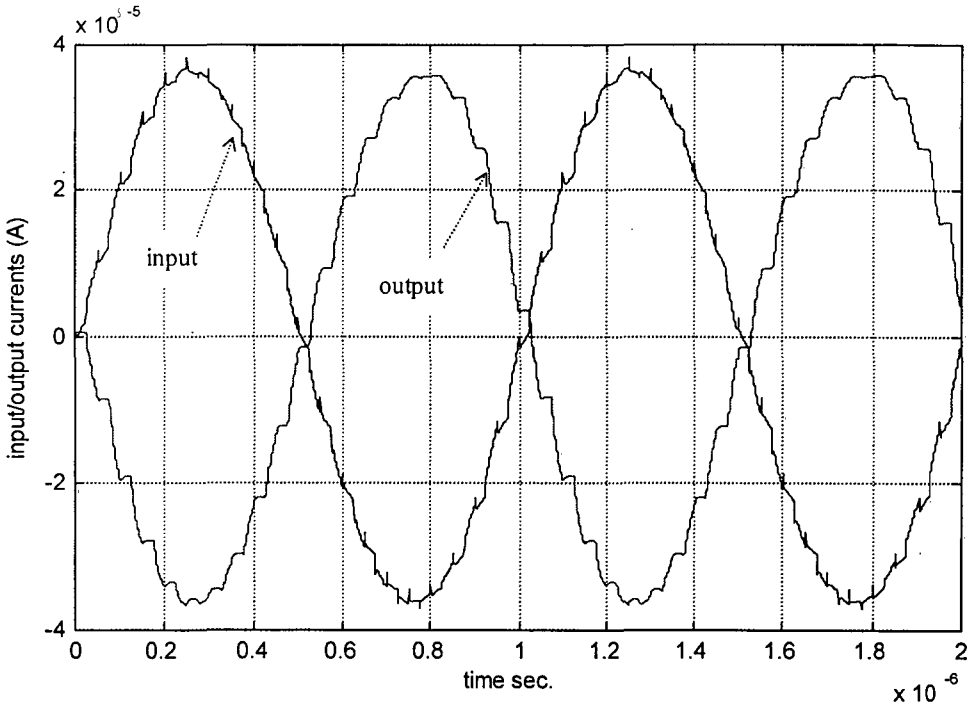


Fig. 4.4. The sinusoidal response of the sample-hold circuit.

4.3 A FULLY BALANCED SWITCHED-CURRENT SAMPLE-HOLD CIRCUIT

Fully Balanced Circuits (FBCs) are widely used in analog-signal-processing applications because they ensure high power supply rejection, improve linearity and increase the dynamic range. Also, in sampled-data circuit (switched-capacitor or switched-current), FBC reduce the effects of charge injection.

In this section, we propose a fully balanced switched-current sample-hold circuit based on the switched-current technique described in [21], which is appropriate for low voltage operation. The programmability of the sample-hold circuit is achieved via the MOSFET Only Current Division (MOCD) technique [33]. Also, we present a new method for the sign-bit realization using the two output currents of the MOCD.

4.3.1 FULLY BALANCED OP-AMP DESIGN

The block diagrams of a single-ended op-amp and a fully balanced one are shown in Fig. 4.5. In fully differential balanced circuits one major problem must be overcome. Because the signals are no longer referred to ground, as in a single-ended circuit, the operating point of the amplifier is not well defined. A Common Mode Feedback Loop (CMFB) block has to be added as shown in Fig. 4.5. (b).

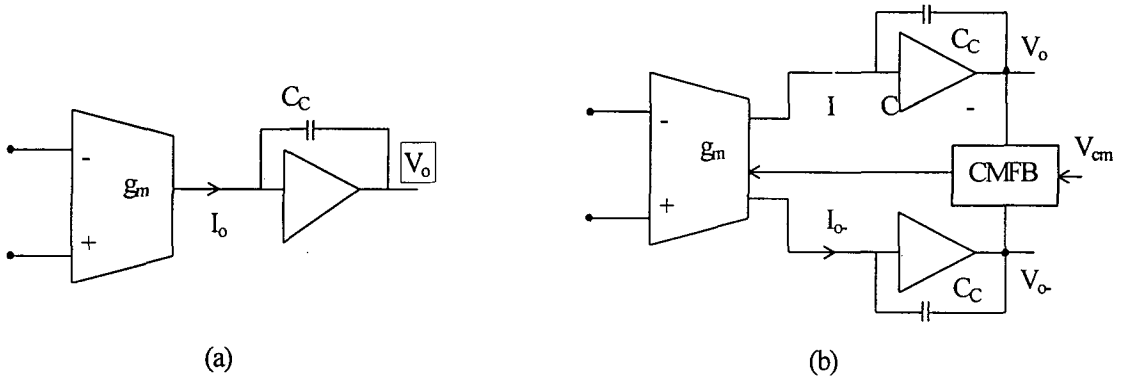


Fig. 4.5. Block diagram of op-amps.
(a) Single-ended.
(b) Fully balanced.

In the switched-current method [21], the MOS transistor is used as a feedback nonlinear resistor as illustrated in Fig.4.6. (a). The common-mode voltage detector is composed of the transistors M_3 and M_4 and operates as follows. Assume the two pairs of transistors (M_1-M_2 and M_3-M_4) to be matched and the input currents (I and –I) to be equal and opposite. The series connected transistors M_3-M_4 ensure that the current through them is the same. The values V_o^+ and V_o^- are generated by equal input currents. Therefore, the value of V_y is equal to V_{CM} since the current through M_3 is the same as the one through M_4.

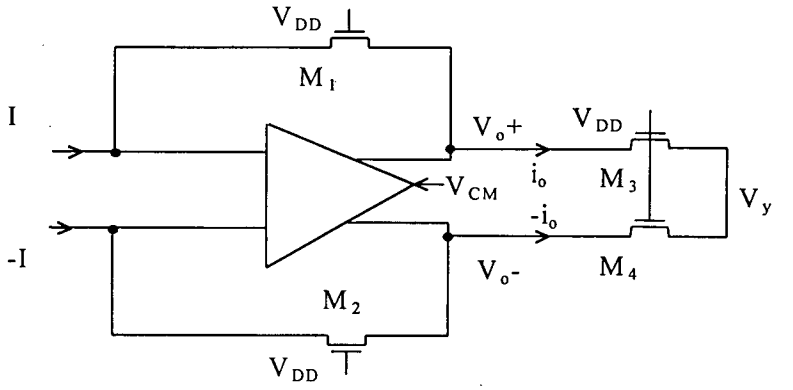


Fig. 4.6. Circuit used to detect the common-mode input voltage.

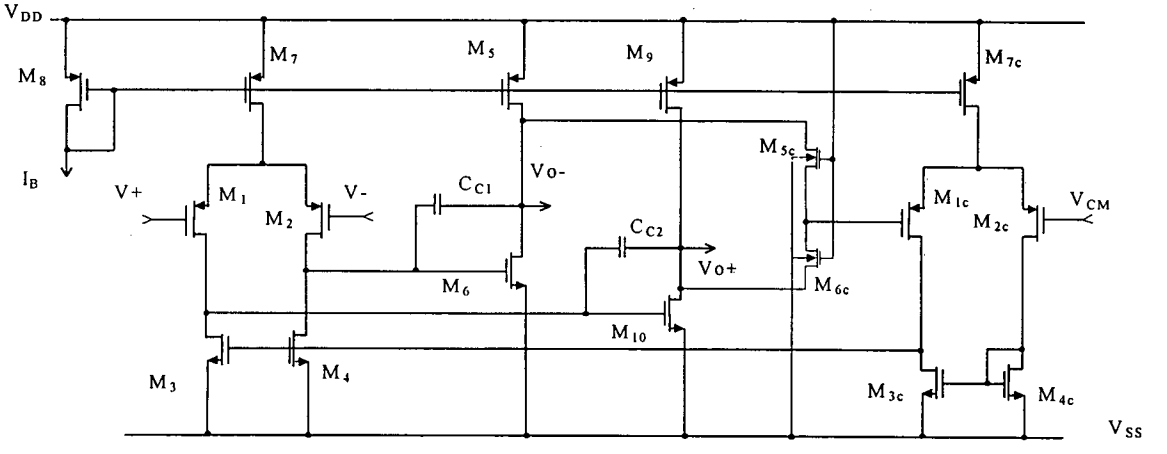


Fig. 4.7. Fully balanced op-amp schematic.

For the SI method [21], at 20 MHz clock, the op-amp specifications can be as those illustrated in Table 4.2. Transistor dimensions and bias currents are calculated using the methodology shown in Appendix B. The design parameters are shown in Table 4.3. The design results are presented in Table 4.4. The op-amp in column 2 is a buffer for a 20pF load. The op-amp illustrated in Fig. 4.7 has been simulated using T-Spice [49]. The simulated AC and DC responses of the op-amp are shown in Fig.4.8.

Table 4.2. Specifications of the op-amp.

Parameter	Value
Supply voltage	±1.5 V
Open loop gain	>40 dB
GB(Gain Bandwidth Product)	~100 MHz
Phase Margin	>50°
Load resistance (R_L)	9 KΩ
Load capacitance (C_L)	2 pF

Table 4.3. Design parameters of the op-amp and simulated specifications.

C_c =0.5pF	P2/GB =5
g_{mI}= 315μA/V	g_{mII}=6.3μA/V
I_{SQN}= 36 nA	I_{SQP}=12 nA
K_p= 35 μA/V^2	K_n= 95 μA/V^2

Table 4.4. Channel widths and simulation results (L=2μm).

Op-amp	1	2
C_L (pF)	2	20
i_{f6}^*	219	219
i_{f1}^*	60	60
i_{f5}^*	595	595
I_B (μA)	120	120
I_{total}(mA)	2.0	28
CEF*	36	49
$W_{1,2,1c,\ 2c}$ (μm)	150	1500
$W_{3,4}$(μm)	30	300
W_8 (μm)	30	30
$W_{7,7c}$(μm)	30	300
$W_{3c,4c}$ (μm)	30	300
$W_{5,9}$ (μm)	200	3000
$W_{6,10}$ (μm)	400	6000
$W_{5c,\ 6c}$ (μm)/L(μm)	5/5	5/5
A_o (dB)	62	75
GB (M Hz)	99	97
Phase margin	54°	50°
C_c	0.5pF	5pF

- I_{norml}=57.8 μA (GB ≅100M Hz, C_L=2pF and i_f =3)

* The definitions are in Appendix A

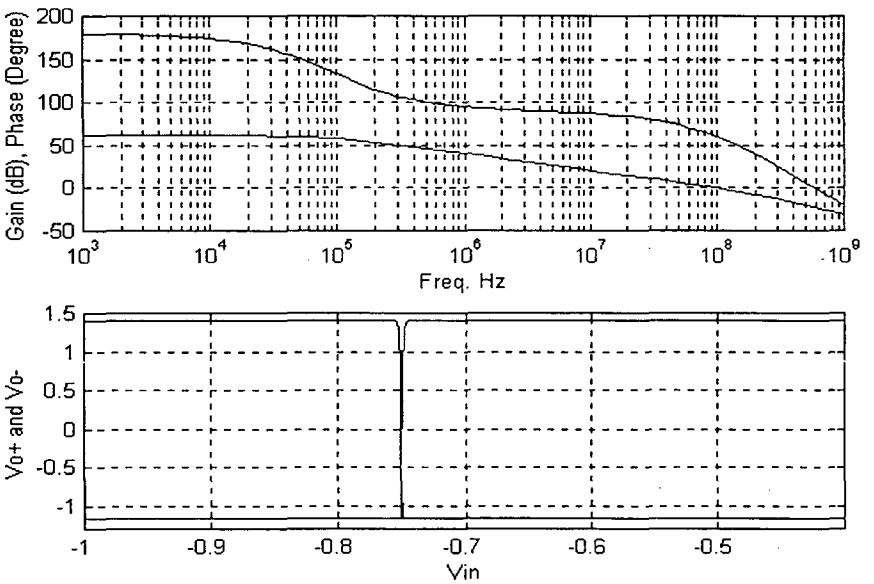


Fig. 4.8. The frequency and DC responses of the balanced op-amp.

4.3.2 FULLY BALANCED SI SAMPLE-HOLD CIRCUIT ARCHITECTURE

A fully balanced switched-current block has been designed using the same thoughtway of the methodology in [21]. The proposed fully balanced (FB) sample-hold is shown in Fig. 4.9. In this circuit, the currents (I and -I) are processed in two steps:

- Track mode: the input currents are fed to the cell when both switches are closed. The currents are memorized as voltages across the holding capacitors. It should be emphasized that linear capacitors are not needed to store the data.
- Hold mode: when the switches open, the voltages are held on the capacitors. These voltages maintain the output currents equal in magnitude and opposite to the input currents as long as M_1 and M_2 have the same aspect ratios.

In the SI structure shown in Fig. 4.9, all the switches operate at a constant DC voltage, equal to V_{CM}, thus causing both the charge injection and settling time [50] to be signal-independent. Moreover, if a proper biasing circuit as the one shown in [21] is used to generate V_{CM}, the gap of the switches [8, 10] is avoided.

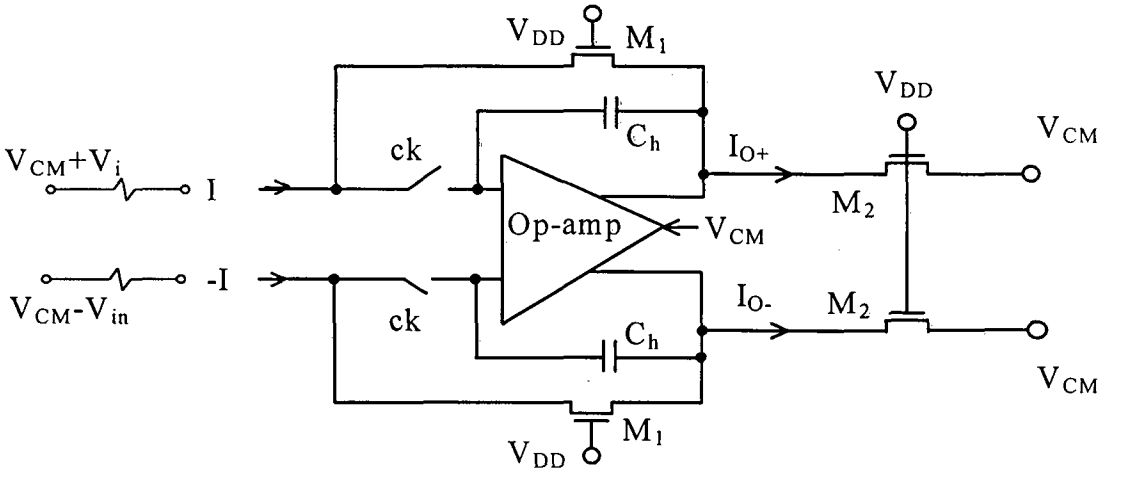


Fig. 4.9. Fully balanced sample-hold circuit.

The circuit shown in Fig.4.9 has been simulated for 3μm/0.8μm nMOS switches, aspect ratios of M_1 and M_2 equal to 6μm/5μm and 0.5pF holding capacitors. Linear resistors are used to convert the input voltages to currents. The responses of the fully balanced SI sample-hold circuit to both sinusoidal and step inputs are shown in Fig.4.10. The simulation shows that the circuit has 1% settling time around 24nsec.

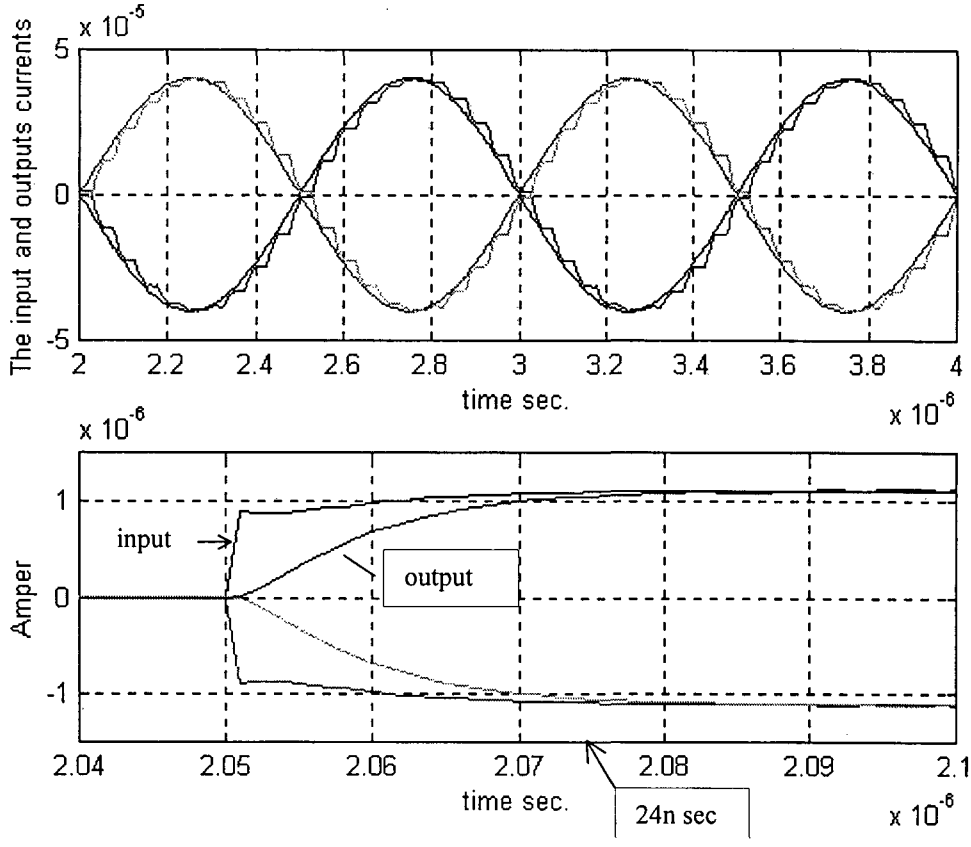


Fig. 4.10. The sinusoidal and step responses of the sample-hold in Fig. 4.9.

4.3.3 SIGN-BIT REALIZATION

The sign-bit realization in [51] is achieved by adding an extra transistor to the MOCD input as shown in Fig. 4.11. This method is based on connecting the MOCD input either to +I or –I, thus changing the direction of the output current to obtain the plus or minus sign. Consequently, all internal potentials of the MOCD change at each

sign-bit variation. Thus, the settling time of the MOCD can affect the maximum allowable clock frequency.

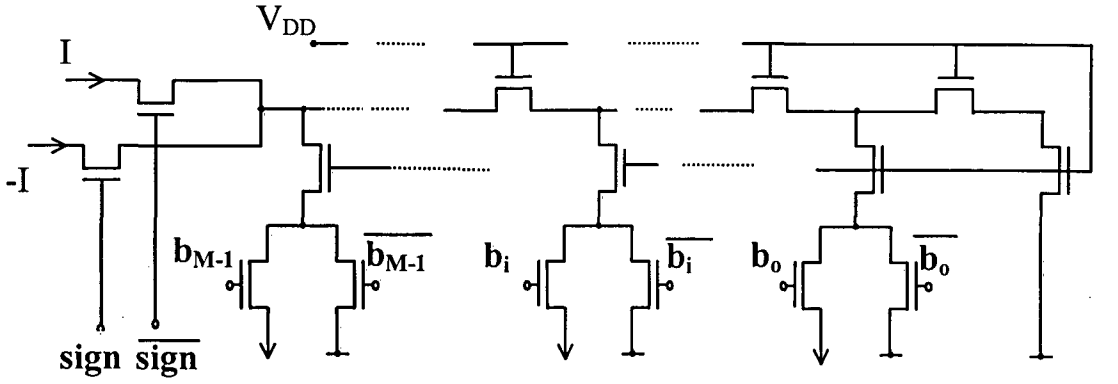


Fig. 4.11. The sign-bit implementation using two MOCD inputs [51].

Here, we propose a new method for the sign-bit realization. This method is suitable for fully balanced circuit where the positive and negative signals are available. The new method uses the two output currents of the MOCD by adding the SUM current of one MOCD to the DUMP current of the other one, as shown in Fig. 4.12. The positive output current I_{o+} is

$$I_{o+} = (2a-1)I = \beta I \tag{4.8}$$

The attenuation factor (a) changes from zero to one when the digital word (<bi>) is changed from 00 to FF (8-bit MOCD). The variation of the coefficient (β) against the control digital word can be represented as in Fig. 4.12. This method avoids the switching method in [51] and no additional circuitry is needed. Moreover, the internal voltages are kept constant when the sign-bit changes. Thus the proposed method is faster than the method that has been used in [51].

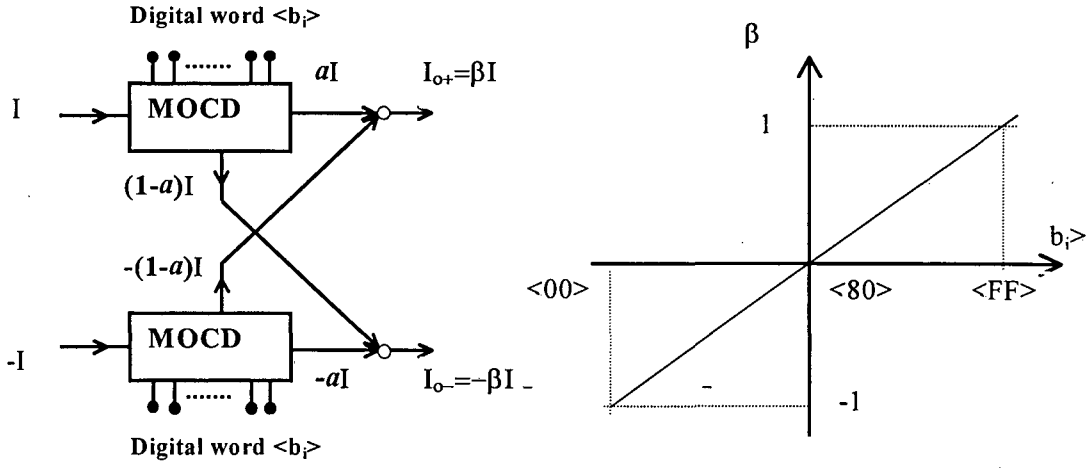


Fig. 4.12. Proposed method for sign-bit realization.

4.3.4 PROGRAMMABLE FULLY BALANCED SAMPLE-HOLD

Using the circuits proposed in sections 4.3.2 and 4.3.3, a fully programmable balanced SI S/H circuit has been implemented. 8-bit MOCDs have been used. The complete circuit has been simulated with 3μm/0.8μm nMOS switches, the aspect ratio of the transistors equal to 6μm/5μm, 0.5pF holding capacitors and 6μm/2.5μm unit transistor of the MOCD. The strategy for the realization of sign-bit has been tested as shown in Fig. 4.13. The top figure of (4.13) shows the sign-bit while the other MOCD bits are 1000000 (<40>). Thus the attenuation factor is ±0.5 as shown in the two bottom curves. Fig. 4.13 displays the expected behavior.

4.4 INTERFACE BLOCKS

The general block diagram of a current-mode signal processing is depicted in Fig. 4.14. The input and output blocks are interfaces between the core section (current-mode) and the surrounding voltage-mode circuit. Moreover, single-to-balanced and balanced-to-single-ended sections are necessary to interface a balanced circuit to a single-ended one.

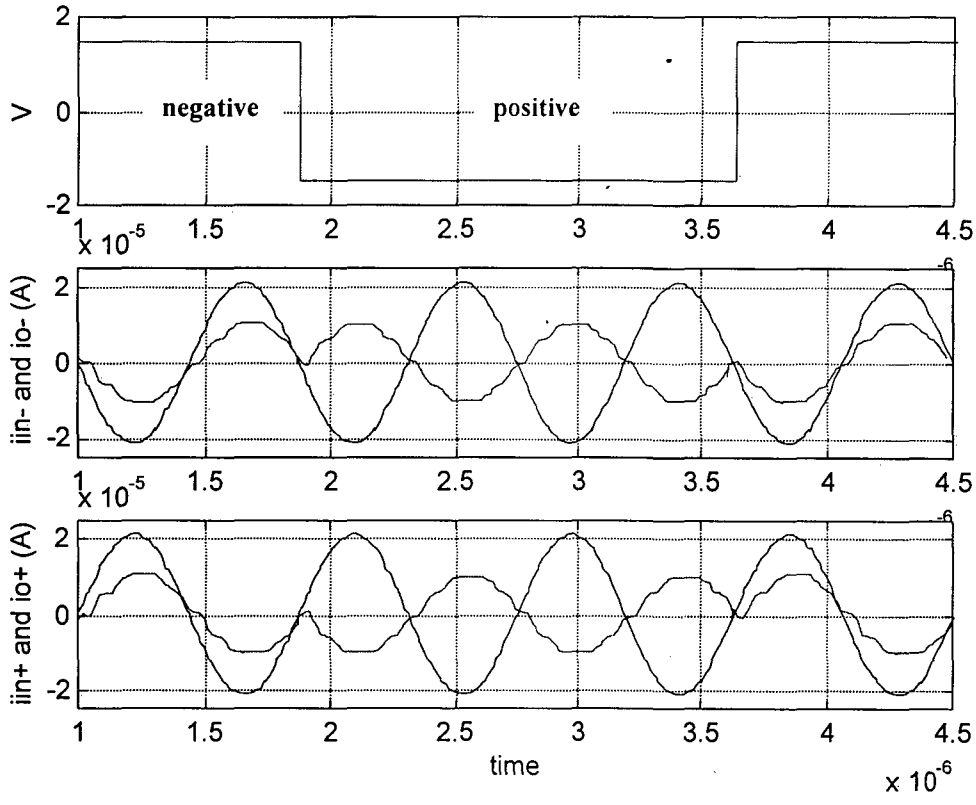


Fig. 4.13. The time response of the programmable SI sample-hold circuit.

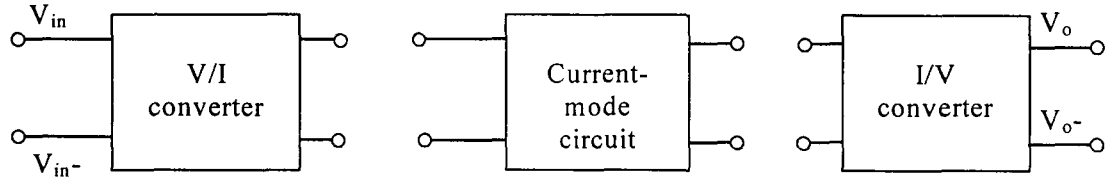


Fig. 4.14. Block diagram for current-mode signal processing.

Fully balanced switched-current circuits often need other auxiliary blocks to interface the current-mode and the voltage-mode circuits. Generally, in fully balanced circuit, the first block is a single-ended input to balanced output block. After that, this voltage signal must be converted to current.

4.4.1 SINGLE-ENDED INPUT TO BALANCED-OUTPUT CONVERTER

In the technical literature, there are some circuits [52, 53] for single-ended to balanced conversion. In this work, the circuit shown in Fig. 4.15 is used to implement

the single-ended to balanced converter [52]. Table 4.5 presents the dimension of the MOS transistors in Fig. 4.15. Fig. 4.16 shows the frequency and DC responses. The 3 dB cutoff frequency is around 10 MHz.

Table 4.5. Channel widths (L=3μm).

$M_1, M_2, M_7, M_8, M_9, M_{11}, M_{12}, M_{13}, M_{b2}$	*4*μm
M_3, M_4, M_{b3}	*8*μm
M_6, M_5, M_{10}, M_{b1}	*20*μm
Total current	*72μA*

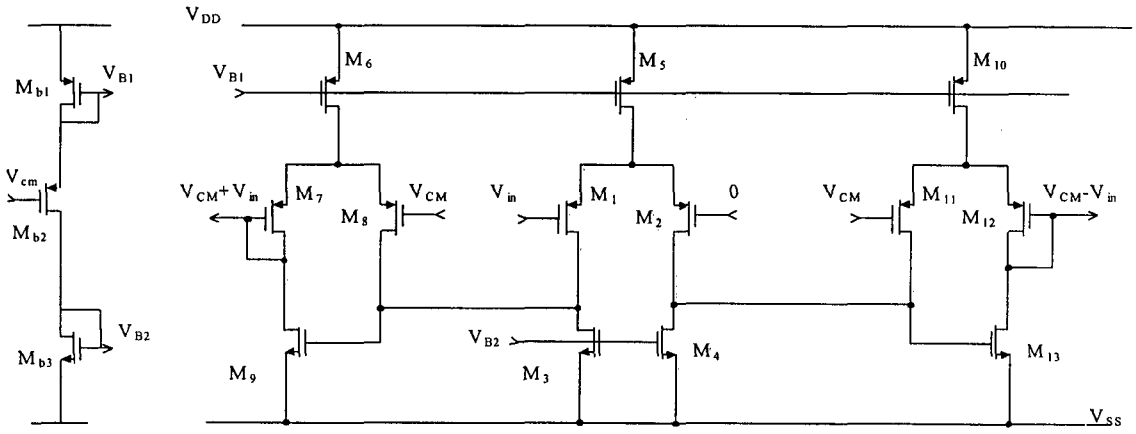


Fig. 4.15. Differential-input to balanced-output converter [52].

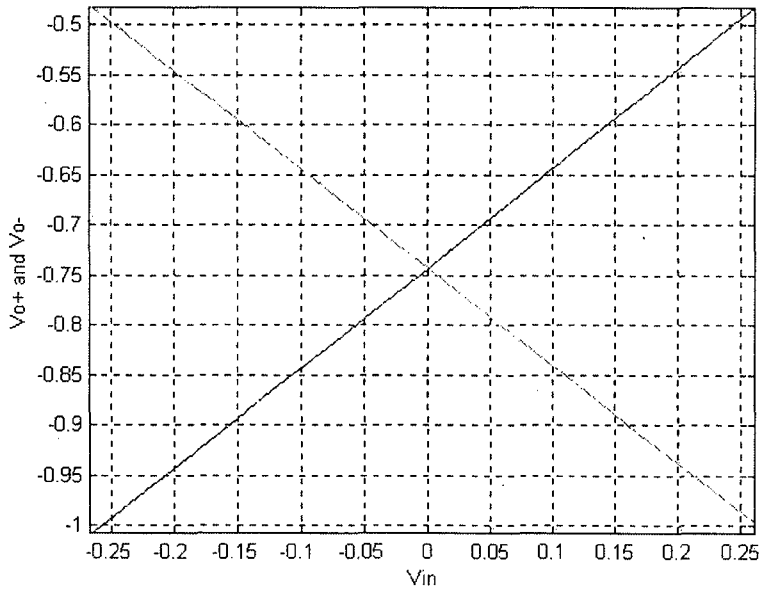


Fig. 4.16.(a). The DC response of the circuit shown in Fig. 4.15.

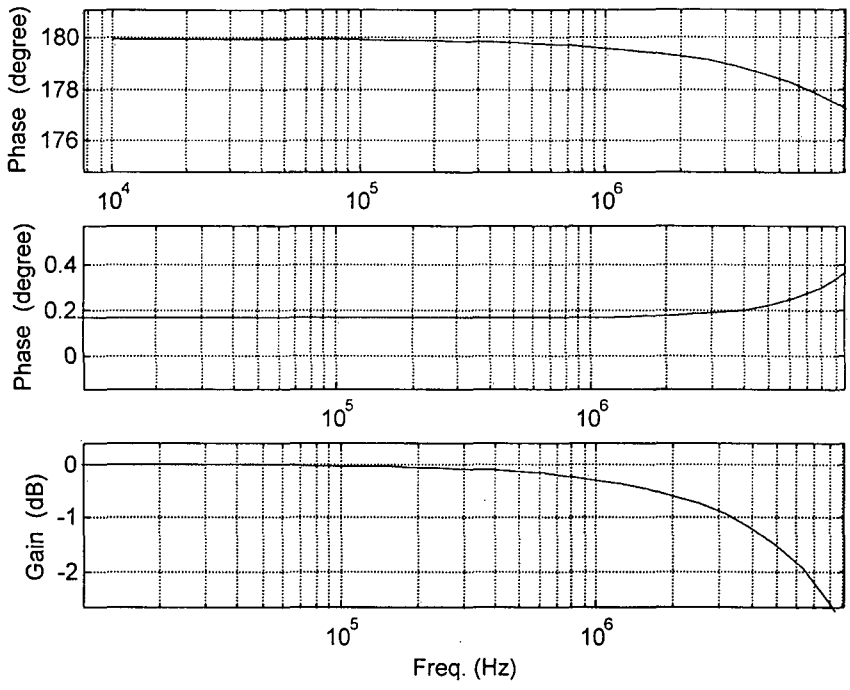


Fig. 4.16.(b). The frequency response of the circuit shown in Fig. 4.15.

4.4.2 VOLTAGE-TO-CURRENT AND CURRENT-TO-VOLTAGE CONVERTERS

In this work, polysilicon resistors (R) are used to perform the linear voltage to current and current to voltage converters, as shown in Fig. 4.17

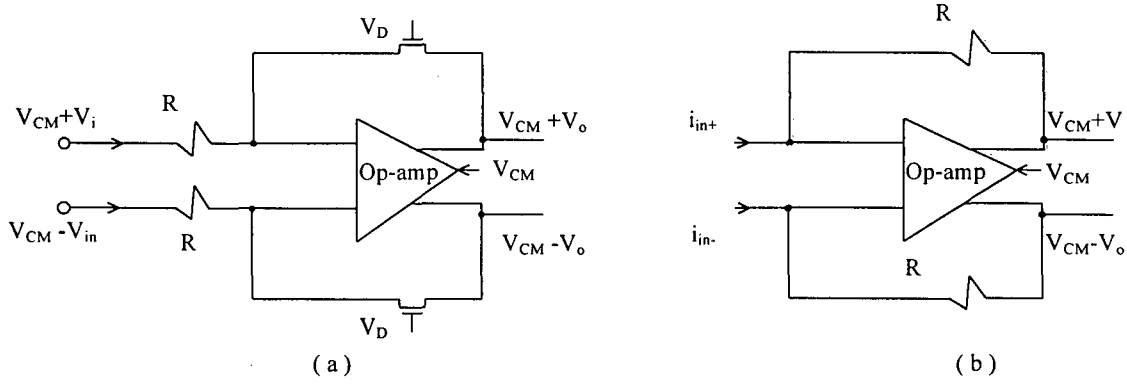


Fig. 4.17. (a) V/I converter. (b) I/V converter.

CHAPTER 5

CIRCULATING FINITE IMPULSE RESPONSE (FIR) FILTER -ARCHITECTURE AND IMPLEMENTATION

5.1 INTRODUCTION

The limited bandwidth of communication channels and multi-path reflections cause inter-symbol interference (ISI). The ISI limits the density of many storage systems and the speed of many communication systems. A finite impulse response (FIR) filter can be used to implement the inverse transfer function of the channel and thus equalize the frequency response. The input-output relationship of an FIR filter is given by

$$y(n) = \sum_{k=0}^{N-1} h_k x(n-k) \tag{5.1}$$

Analog tapped-delay line has been used for the FIR filter realization [54] as shown in Fig. 5.1. As shown in this figure, the signal is delayed with added transition errors (sampling errors) which are known as multiple re-sampling errors. A significant increase in the FIR performance can be gained if the system design avoids the re-sampling errors of the traditional analog delay line. For this purpose, the circulating technique [55] for FIR filter realization has been proposed.

5.2 APPLICATIONS

The Decision Feedback Equalizer (DFE) has been used for ISI cancellation thus increasing the speed of data transmission [56] and the storage capability [57, 58, 59].

Generally, the two main components of the DFE are a forward equalizer and a feedback equalizer that eliminate the ISI before and after each symbol, respectively.

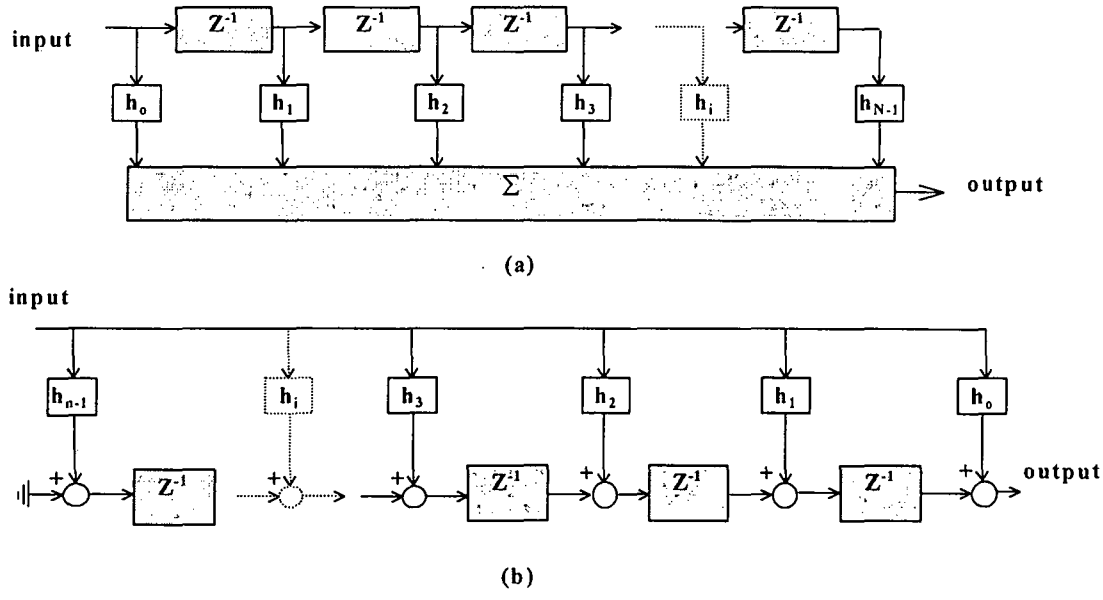


Fig. 5.1. Realization forms of the analog delay line.

(a) Direct-form realization.

(b) Transposed form realization.

Modern magnetic storage channels, which usually use the partial response maximum likelihood (PRML) detection method, require an adaptive equalizer for the reduction of ISI [57, 58, 59]. Also, for time-variant channel characteristic (such as mobile wireless communication), the adaptive DFE is necessary to compensate the channel variation. The general block diagram of the adaptive DFE is shown in Fig. 5.2. The forward and backward equalizers are realized using fully programmable FIR filters. In this work, we introduce a fully balanced programmable FIR filter suitable for read channel disk-drive and for mobile wireless communications applications at low supply voltage.

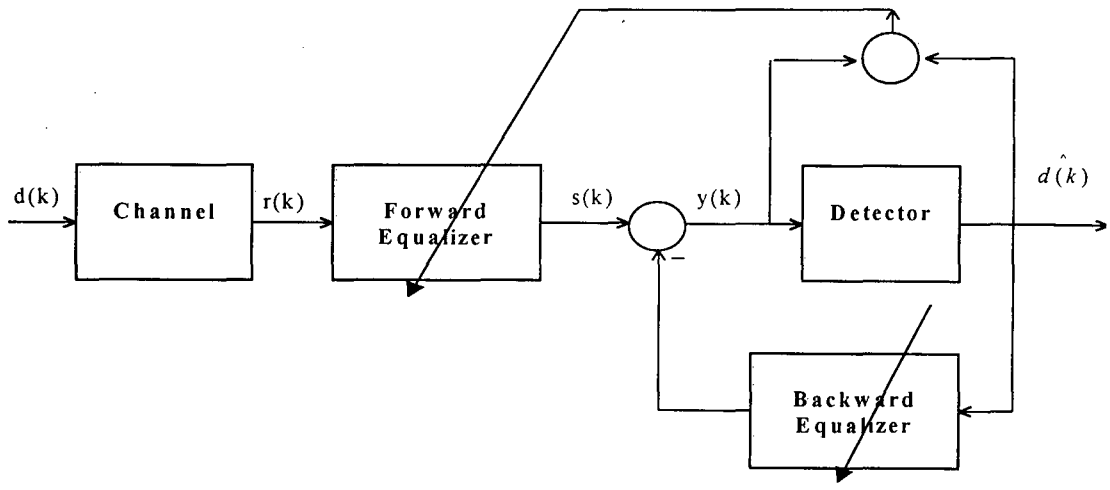
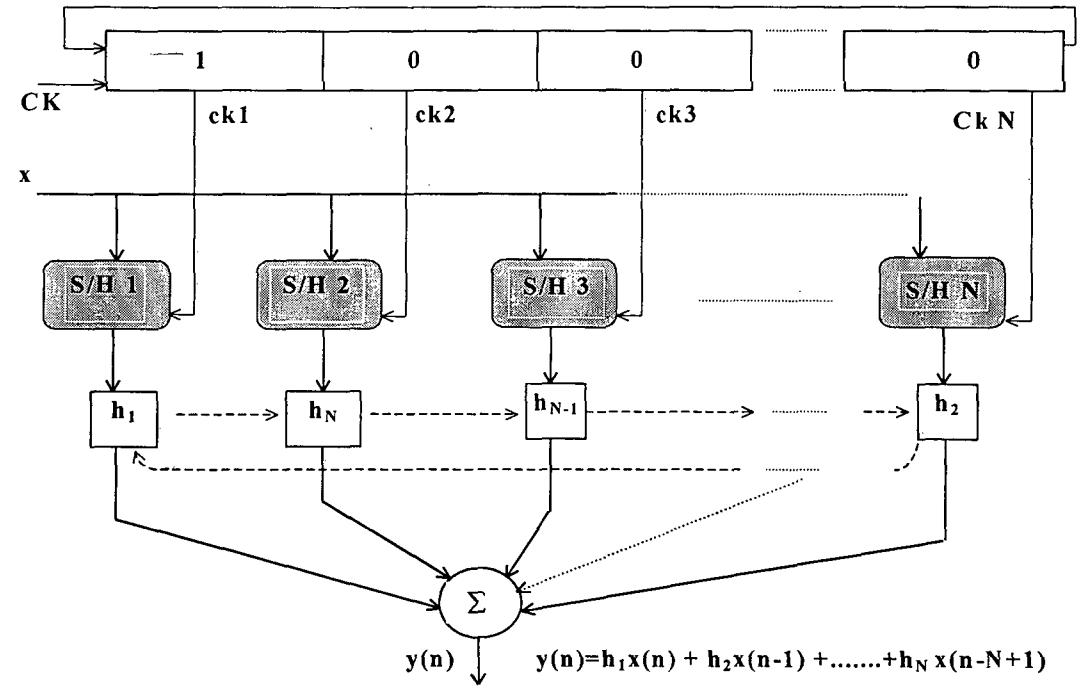


Fig. 5.2. Block diagram of an adaptive DF equalizer.

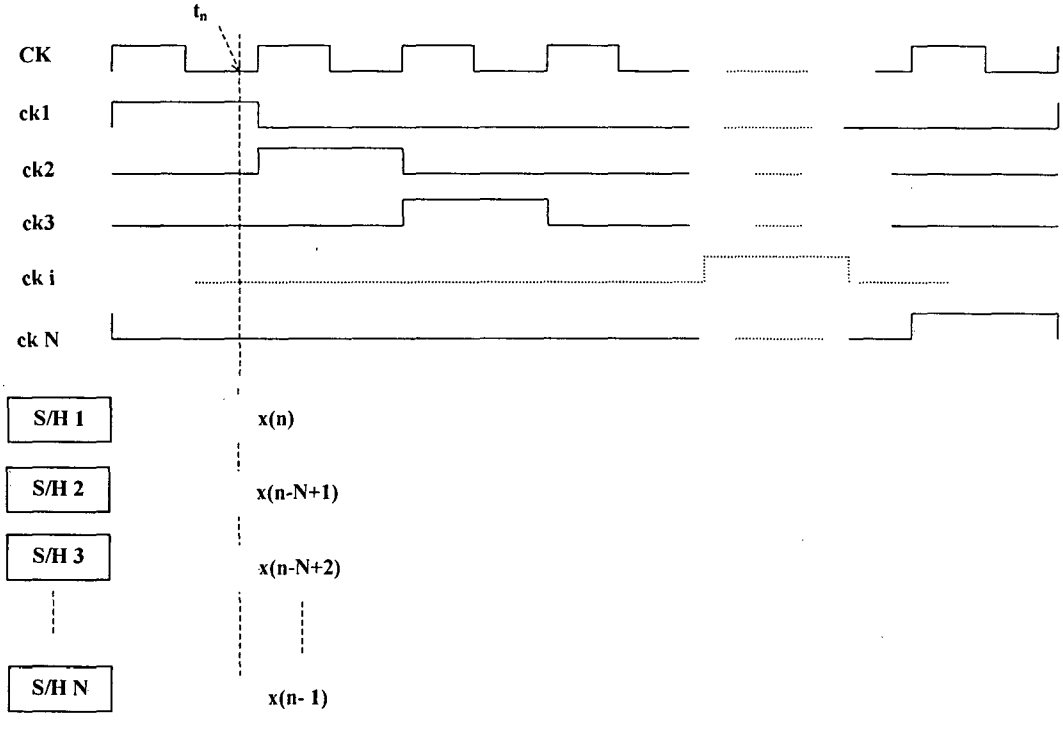
5.3 CIRCULATING FORM OF THE FIR FILTER

The circulating form of the FIR filter is shown in Fig. 5.3.(a). Each S/H samples the input signal only once every N clock cycles and holds the signal value for the remaining N-1 cycles. To simulate the analog delay line, h_1 is always associated with the most recent sample (denoted as zero time reference), h_2 associates with S/H that has been sampled at -T from the reference time, h_3 with the S/H that has been sampled at –2T and so on. So, the coefficients of the FIR filter must rotate one position for each clock phase as shown in Fig. 5.3.(a). The clock phases are illustrated in Fig. 5.3.(b).

The circulating technique simulates a tapped delay line without passing the sampled value into series delay taps on each clock cycle. Consequently, this structure has the advantage of avoiding the propagation of the re-sampling errors from each cell to the following. Table 5.1 illustrates the details of the signal and the distribution of coefficients for the first N clock cycles [51]. Moreover, Table 5.2 shows the signal and coefficients after the first N clock cycles. Also Tables 5.1 and 5.2 show the static property of the stored signal in S/H's and the dynamic property of the FIR coefficients.



(a)



(b)

Fig.5.3. General schematic of an N-tap FIR filter.

(a) Circular FIR filter structure (coefficients during ck1).

(b) The control clocks and the currents of the S/H's at t_n.

Table 5.1. Stored signals and distribution of coefficients through the first N clock cycles.

Time		S/H 1		S/H 2		S/H 3		.....	S/H N		O/p
		Data	**Coef.**	**Data**	**Coef**	**Data**	**Coef.**	.....	**Data**	**Coef.**	
0T	(ck1)	x_0	h_1	-----	-----	---	------	.....	-------	-------	y_0
1T	(ck2)	x_0	h_2	x_1	h_1	----	------	.....	-------	-------	y_1
2T	(ck3)	x_0	h_3	x_1	h_2	x_2	h_1	.....	-------	-------	y_2
3T	(ck4)	x_0	h_4	x_1	h_3	x_2	h_2	.....	-------	-------	y_3
.....		x_0	....	x_1	h_4	x_2	h_3	.....	-------	-------	.....
.....		x_0	..	x_1	....	x_2	h_4	.....	-------	-------	.....
.....		x_0	....	x_1	..	x_2	....	.....	-------	-------	.....
(N-1)T	(ck N)	x_0	h_N	x_1	h_{N-1}	x_2	h_{N-2}	.....	x_{N-1}	h_1	y_{N-1}

Table 5.2. Stored signals and distribution of coefficients after the first N clock cycles.

Time		S/H_1		S/H_2		S/H_3		.....	S/H_N		O/P
		Data	**Coef**	**Data**	**Coef**	**Data**	**Coef**	.....	**Data**	**Coef.**	
NT	**(ck1)**	$\underline{x_N}$	$\underline{h_1}$	x_1	h_N	x_2	h_{N-1}	.....	x_{N-1}	h_2	y_N
(N+1)T	(ck2)	x_N	h_2	$\underline{x_{N+1}}$	$\underline{h_1}$	x_2	h_N	.....	x_{N-1}	h_3	y_{N+1}
(N+2)T	(ck3)	x_N	h_3	x_{N+1}	h_2	$\underline{x_{N+2}}$	$\underline{h_1}$	.....	x_{N-1}	h_4	y_{N+2}
(N+3)T	(ck4)	x_N	h_4	x_{N+1}	h_3	x_{N+2}	h_2	.	x_{N-1}	h_5	y_{N+3}
.....		x_N	....	x_{N+1}	h_4	x_{N+2}	h_3	.....	x_{N-1}	.....	.....
.....		x_N	..	x_{N+1}	....	.....	h_4	.....	x_{N-1}	.....	.....
		x_N	....	x_{N+1}	..	.....	....	.....	x_{N-1}	.....	.....
(2N-1)T	(ckN)	x_N	h_N	x_{N+1}	h_{N-1}	x_{N+2}	h_{N-2}	.....	$\underline{x_{2N-1}}$	$\underline{h_1}$	y_{2N-1}

5.4 DIGITAL CONTROL CIRCUITS

As previously shown, the FIR coefficients must rotate one position after each clock cycle. The rotating switch matrix [60] was used to achieve this function. In this work, the FIR filter coefficients are controlled by the MOCD and the rotating switch matrix is simulated by rotating the control digital words <bi> of the MOCDs. The circulating process can be achieved using combinational or sequential logic circuit. Firstly we used the combinational logic circuit to circulate the coefficients. Fig. 5.4 shows the one-bit circulating circuit. Thus, for each M-bit MOCD, M blocks must be used to circulate the coefficients.

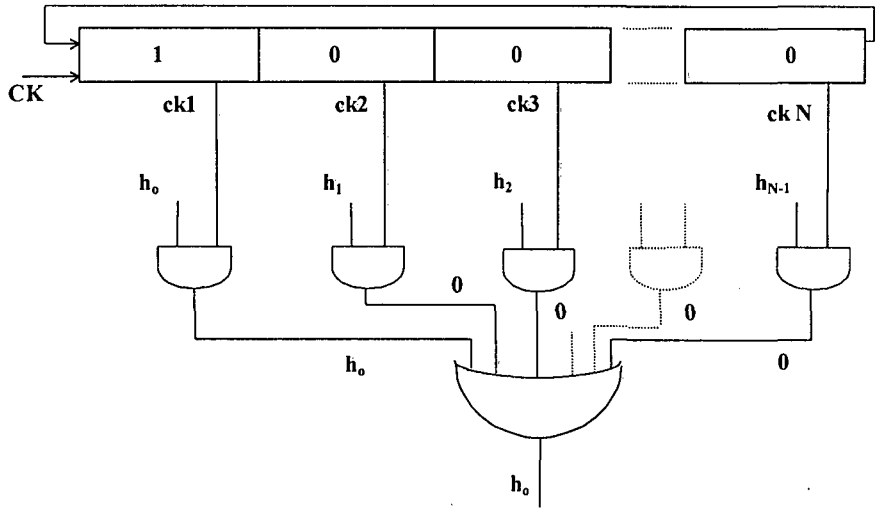
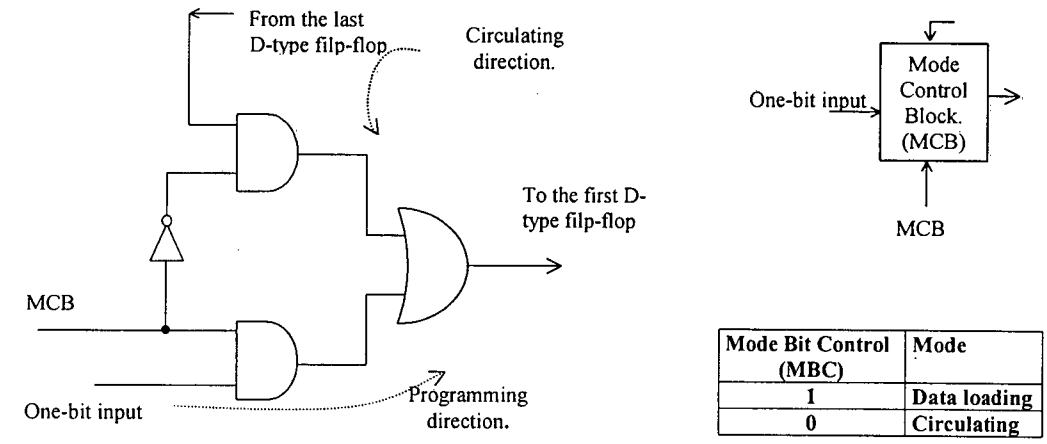


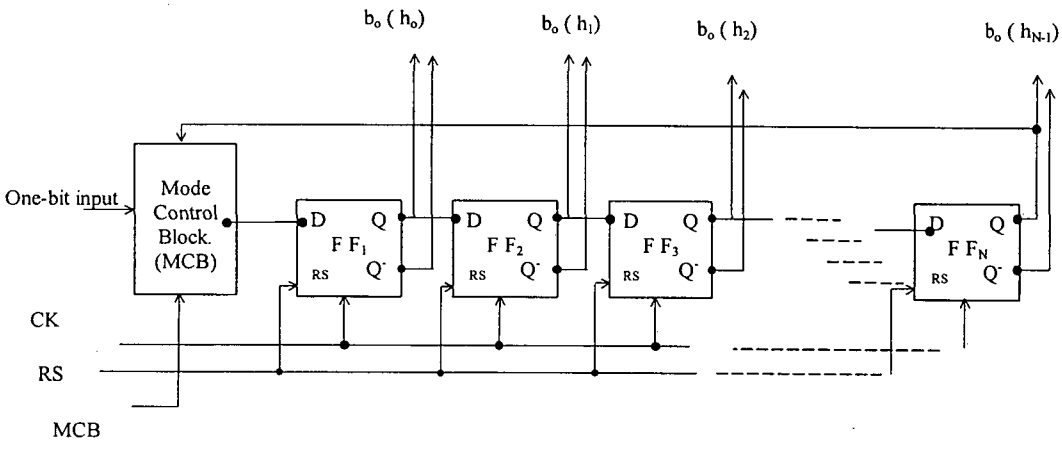
Fig. 5.4. The schematic of the one-bit circulating circuit.

The shifting process of the FIR filter coefficients can be achieved using shift registers. To reduce the total number of pads, the shift register has been used to load the data serially. So another circuit is necessary to select the operating mode, loading (programming) or circulating, as shown in Fig. 5.5.(a). The complete one-bit circulating block is depicted in Fig.5.5.(b). Also, the clock phases (ck1, ck2,.....ckN) are generated by using cascaded D-type flip- flops as shown in Fig. 5.6. The RS terminal is necessary to set the initial word to 100000.... and then circulate it.



Mode Bit Control (MBC)	Mode
1	Data loading
0	Circulating

(a)



(b)

Fig. 5.5. The sequential control circuit.

(a) The mode control block.

(b) One-bit circulating block (b_o).

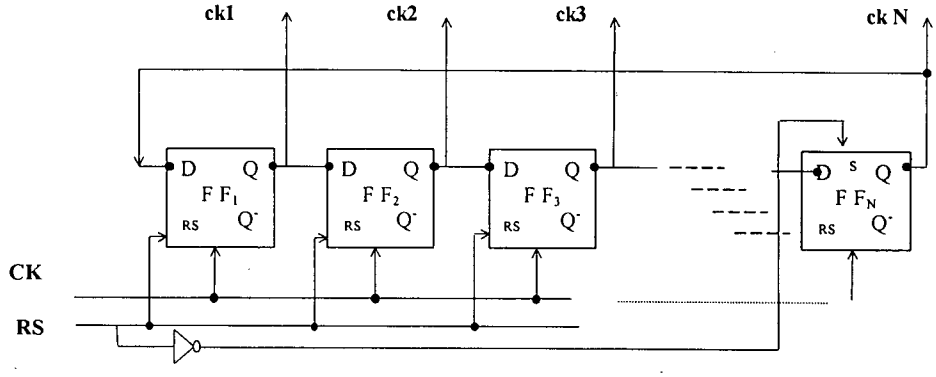


Fig. 5.6. Clock generator.

5.5 SWITCHED-CURRENT REALIZATION OF THE CIRCULATING FIR FILTER

In this section, we present the design of two FIR filters. A 4-tap single-ended FIR filter and a fully balanced 8-tap filter are presented. They can be used for time recovery [56] and disk drive applications, respectively.

5.5.1 SINGLE-ENDED 4-TAP SWITCHED-CURRENT FIR FILTER

The S/H circuit and the programmable MOCD has been used for the SI implementation of a 4-tap circular FIR filter as shown in Fig. 5.7.(a). The front-end section is a linear voltage-to-current converter. After the V-I conversion, the signal is fed to the S/H's according to the timing diagram shown in Fig. 5.7.b. The stored signals, multiplied by their corresponding coefficients, are summed in the output section, which is a linear current-to-voltage converter.

In practice, an internal MOCD operates as a (large area) switch (M_{3L} Fig. 5.8). Thus, a significant amount of charge can be transferred to the holding capacitor due to both the channel charge and the capacitive coupling between gate and source. Fig. 5.8. (a) illustrates details about the switching methodology of the FIR filter structure shown in Fig. 5.7. (a), at clock cycle ck1. Generally, the injected charge due to the switch "S2" is minimized by using a CMOS transmission gate or a dummy transistor technique.

Here we propose a clock scheme to reduce the injected charge into the holding capacitor due to MOCD M_{3L}. The scheme is shown in Fig. 5.8. (b). Switch "S2" has to open before M_{3L} turns off to avoid the charge injected by M_{3L} to be stored into the holding capacitor. So, the MOCD clock (ck_{1s}) must be delayed with respect to ck1 as

shown in Fig. 5.8. (b). This delay time must be as short as possible in order to not increase the settling time error.

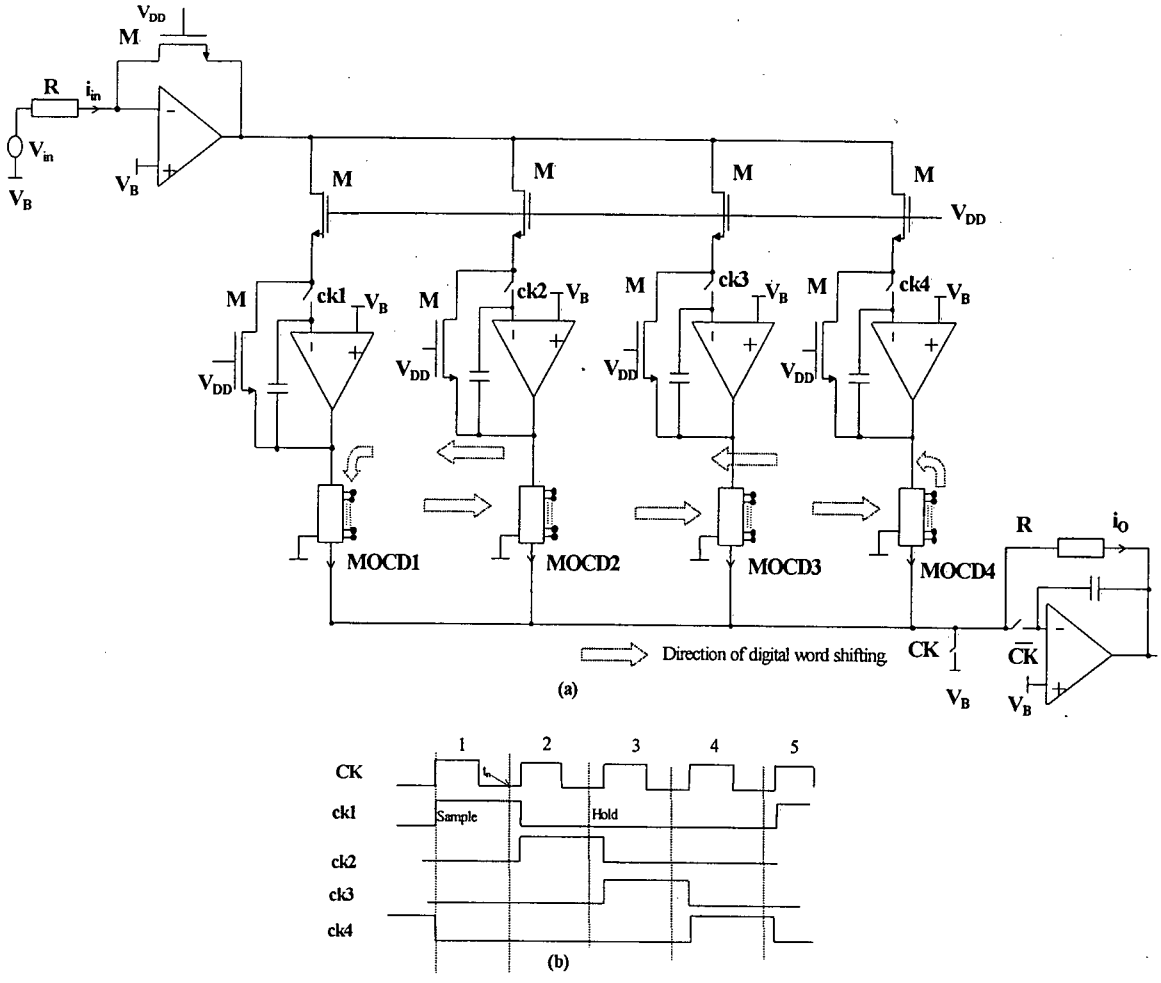


Fig. 5.7. The 4-tap FIR filter in circulating form.

(a) Scheme .

(b) Clock phases.

To validate our analysis, the circuit shown in Fig. 5.8. (a) has been simulated with SMASH [38] for a 10μA input current and using 3μm/0.8μm n-channel switches at 20MHz clock frequency. The ACM MOSFET model [22] has been used for the simulations. M and M_{3L} have aspect ratios equal to 6μm/5μm and the holding capacitor is 0.5 pF. The two-stage CMOS op-amp designed in Appendix B has been used in the simulation. The delay time between the main clock (ck1) and the delayed one ($ck1_s$)

was 0.4nsec, which is equivalent to two cascaded logic inverters from the AMS library of the 0.8μm double-poly double-metal CMOS technology. The circuit has been simulated using both the proposed clock and the conventional clock (without any delay) schemes. The simulation results are depicted in Fig. 5.9. The DC offset current (output-2) is due to the charge accumulation into the holding capacitor which disappears after using the proposed clock.

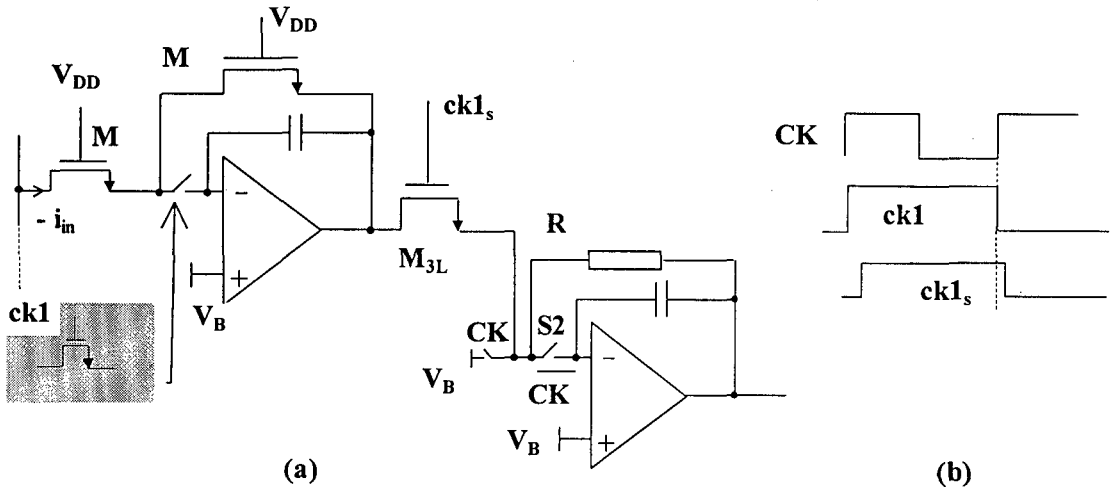


Fig. 5.8. Switching methodology to reduce charge injection.

(a) The basic S/H cell and the summer block.

(b) Proposed clock scheme.

Obs: M_{3L} is equivalent to an MOCD in Fig. 5.7. (a).

The 4-tap filter shown in Fig. 5.7.(a) has been designed and laid out using the Tanner Tools package [49]. L-edit has been used to extract the netlist for the full chip. The FIR filter coefficients have been set to h_1=00, h_2=00, h_3=00, and h_4=3F. These coefficients realize a pure 4-clock cycle delay. The output and input currents are illustrated in Fig. 5.10. The DC offset current and spikes have been suppressed using the clock scheme of Fig. 5.8. (b).

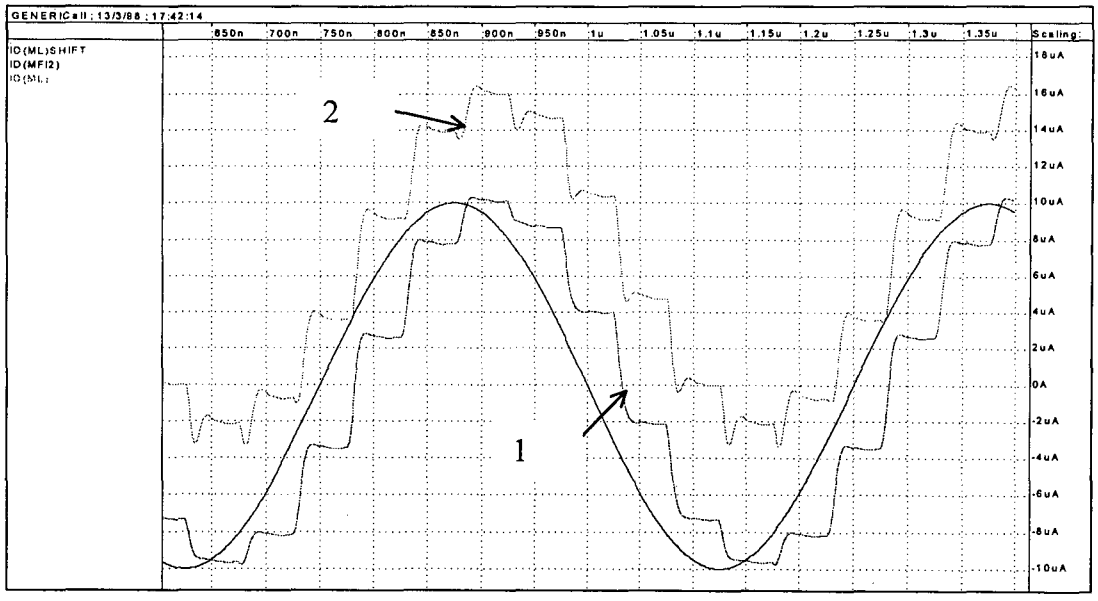


Fig. 5.9. Simulation results for the circuit of Fig. 5.8.

1- Proposed clock. 2- Conventional clock.

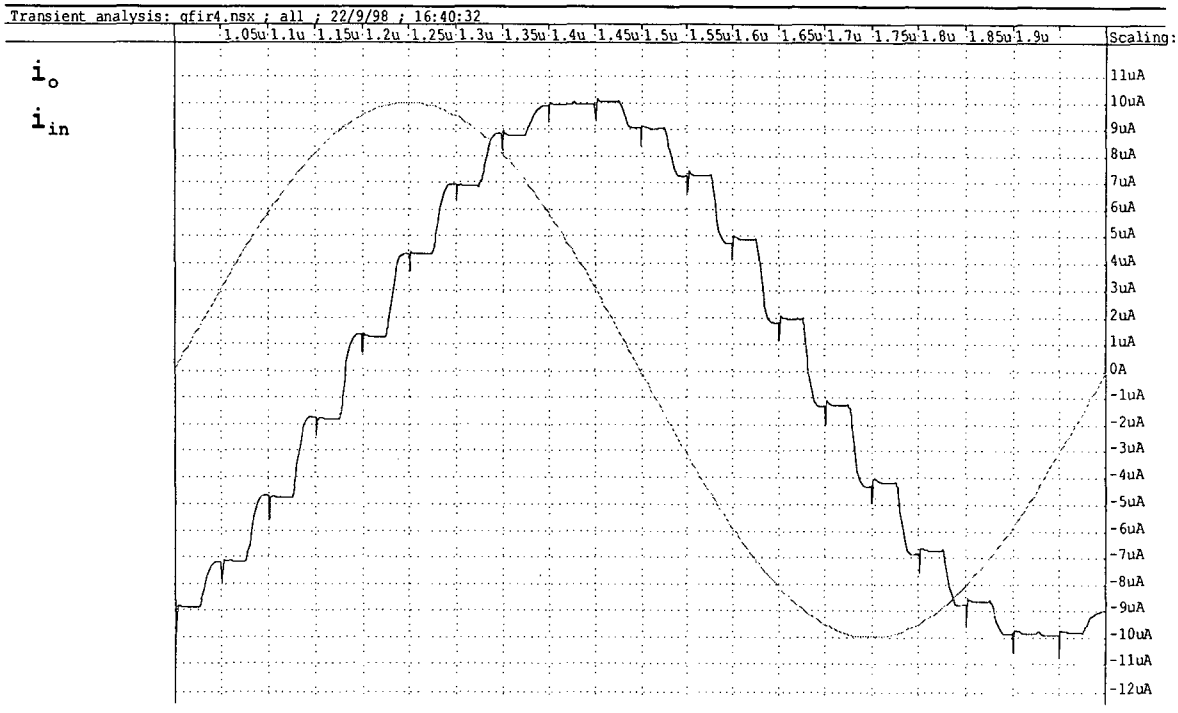
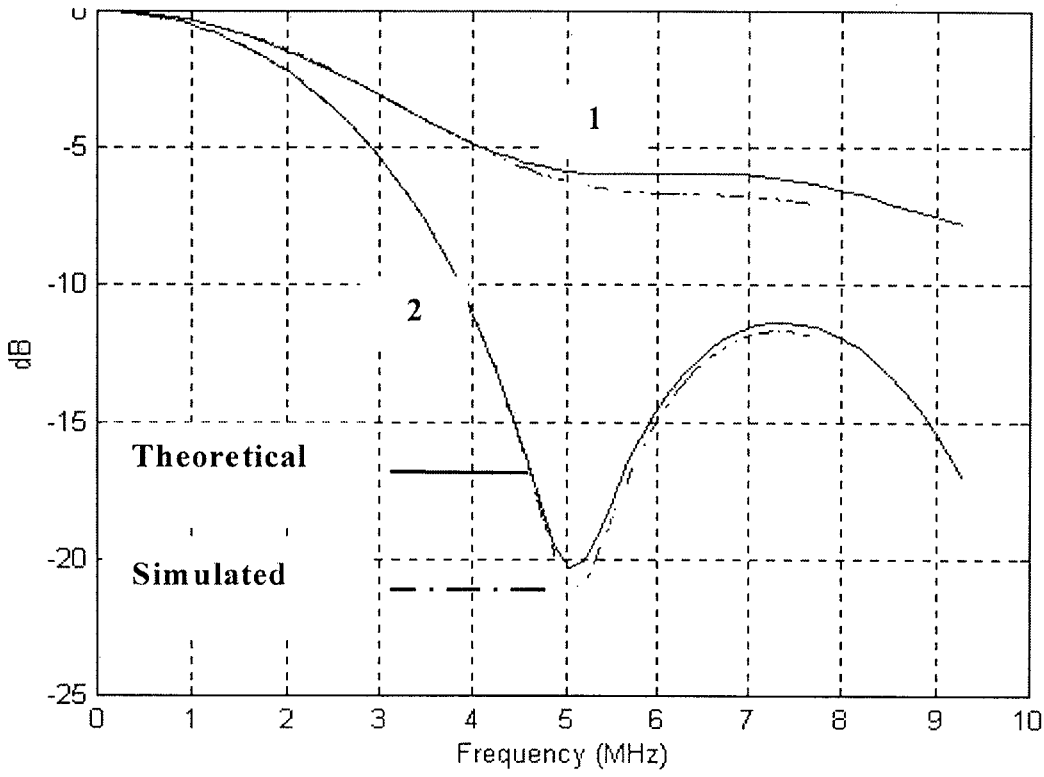


Fig. 5.10. Pure delay of 4 clock cycles (h_1=h_2 = h_3 =00 and h_4 =3F).

T-Spice [49] has been used to obtain the impulse response of the FIR filter for different coefficients (digital words). The MATLAB FFT routine has been used to obtain the frequency response. The theoretical curves have been obtained using the ideal

freqz-routine from the MATLAB package. Fig. 5.11 shows the programmability of the filter for different digital words.

In the SI circuit shown in Fig. 5.7. (a), the currents are continuously fed to all S/H's through the input transistors (M). Thus, for an N-tap FIR filter, the input amplifier (V-I converter circuit) must be able to drive (N+1) transistors.



$h_1 = 3F$, $h_2 = 15$, $h_3 = 0B$ and $h_4 = 06$ (curve 1).

$h_1 = 3F$, $h_2 = 36$, $h_3 = 2E$ and $h_4 = 27$ (curve 2).

Fig. 5.11. The magnitude response of the FIR filter for different digital words.

5.5.2 FULLY BALANCED FIR SWITCHED-CURRENT FILTER

Here we design a fully balanced programmable FIR filter using the circulating technique. An 8-tap FIR filter has been implemented using the fully balanced S/H circuit presented in chapter 4. The switched-current realization of the 8-tap FIR filter is depicted in Fig. 5.12. The figure shows tap number i which is clocked at phase cki.

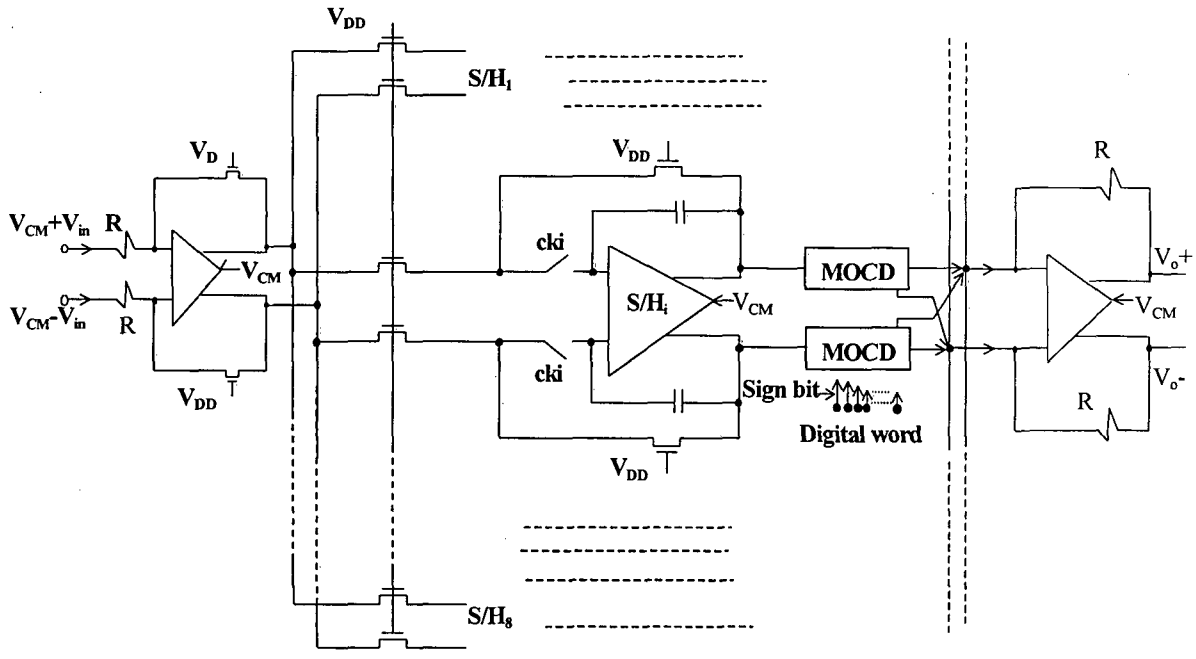


Fig. 5.12. 8-tap fully balanced switched-current FIR filter.

The programmability of the FIR filter has been tested for low-pass and bandpass filters. The filter coefficients have been determined using the Parks-McClellan optimal equiripple FIR filter design from the MATLB package. The coefficients and their equivalent digital words are shown in Table 5.3.

- **SIMULATION APPROXIMATION**

To simplify the overall switched-current circuit for the purpose of simulation, the fully balanced op-amp has been modeled as shown in Fig. 5.13. Each single-ended op-amp is modeled by an ideal voltage-controlled voltage source. Also, to obtain the impulse response, the coefficients have been circulated only through the first MOCD (S/H 1) while the other MOCD's words have been set to (10000000); particularly, the stored data in S/H2,.....and S/H8 are zero.

Table 5.3. The attenuation factors of the MOCDs for low- and bandpass FIR filters.

Coeffs. of low-pass Filter			Coeffs. of bandpass filter-I			Coeffs. of bandpass filter-II		
MATLAB	Digital word	SI*	MATLAB	Digital word	SI*	MATLAB	Digital word	SI*
-0.0698	1 0001000	-0.06	-0.0140	1 0000001	-0.0032	-0.0234	1 0000011	-0.02
0.1142	0 1110001	0.123	-0.2049	1 0011010	-0.200	-0.2031	1 0011010	-0.2
0.2233	0 1100011	0.232	-0.0134	1 0000001	-0.0032	-0.0234	1 0000011	-0.02
0.3254	0 1010110	0.335	0.2128	0 1100100	0.215	0.2187	0 1100100	0.2215
0.3254	0 1010110	0.335	0.2128	0 1100100	0.215	0.2187	0 1100100	0.2215
0.2233	0 1100011	0.232	-0.0134	1 0000001	-0.0032	-0.0234	1 0000011	-0.02
0.1142	0 1110001	0.123	-0.2049	1 0011010	-0.200	-0.2031	1 0011010	-0.2
-0.0698	1 0001000	-0.06	-0.0140	1 0000001	-0.0032	-0.0234	1 0000011	-0.02

* Coefficients of the FIR filters from the SI simulation.

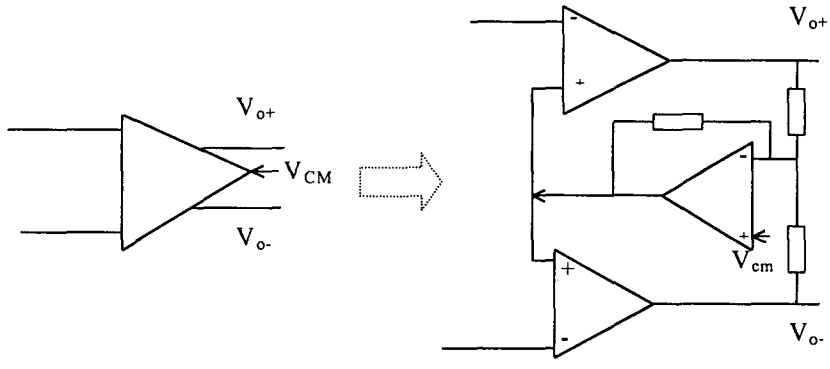


Fig. 5.13. A fully balanced op-amp and its simulated model.

The switched-current FB filter shown in Fig. 5.12 has been simulated to test the programmability for low-pass and bandpass filters. The simulation result (impulse response) has been used to obtain the filter frequency response using MATLAB FFT. Fig. 5.14 and Fig. 5.15 illustrate the ideal (MATLAB result) and simulated (SI filter response) frequency response of the low-pass and bandpass filters, respectively. The feedthrough error due to the internal switching of the MOCD's is canceled out due to the cross connection of the DUM and SUM terminals as shown in Fig 5.12. In Fig. 5.15,

the error between the theory (MATLAB) and simulated result is due to limited resolution of the MOCD (7'bit). This error is reduced as long as the maximum error between the real coefficients and its SI implementation to be minimum, as shown in Fig. 5.16.

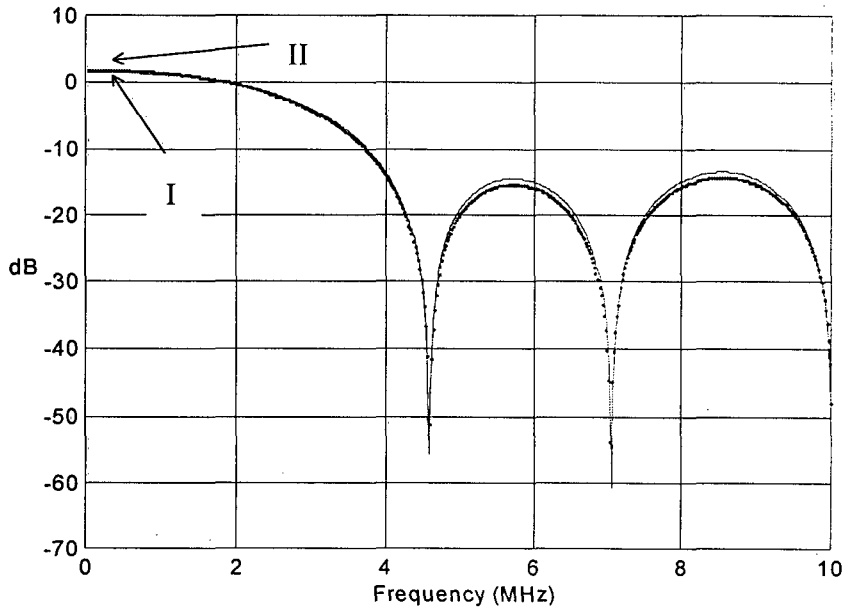


Fig. 5.14. The frequency response of the low-pass filter.
(I) theory and (II) Simulation.

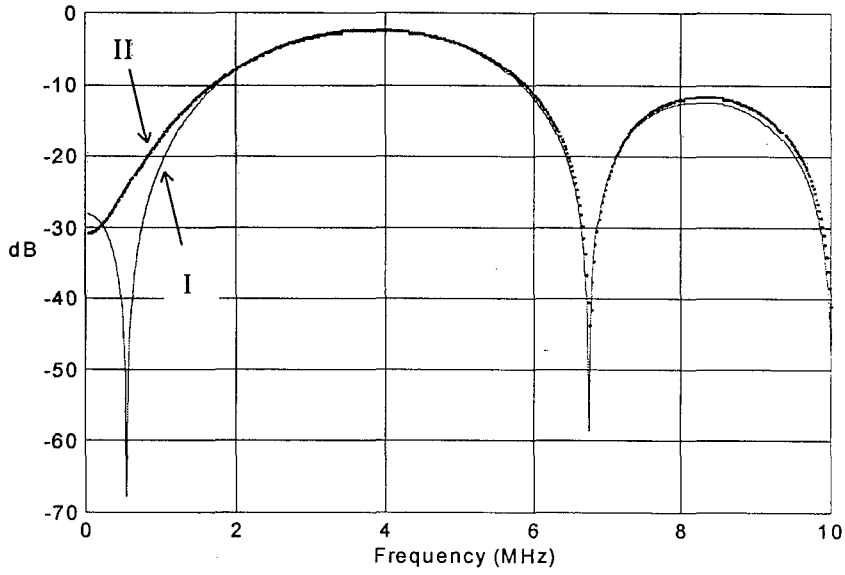


Fig. 5.15. The frequency response of the bandpass filter-I.
(I) Theory and (II) Simulation.

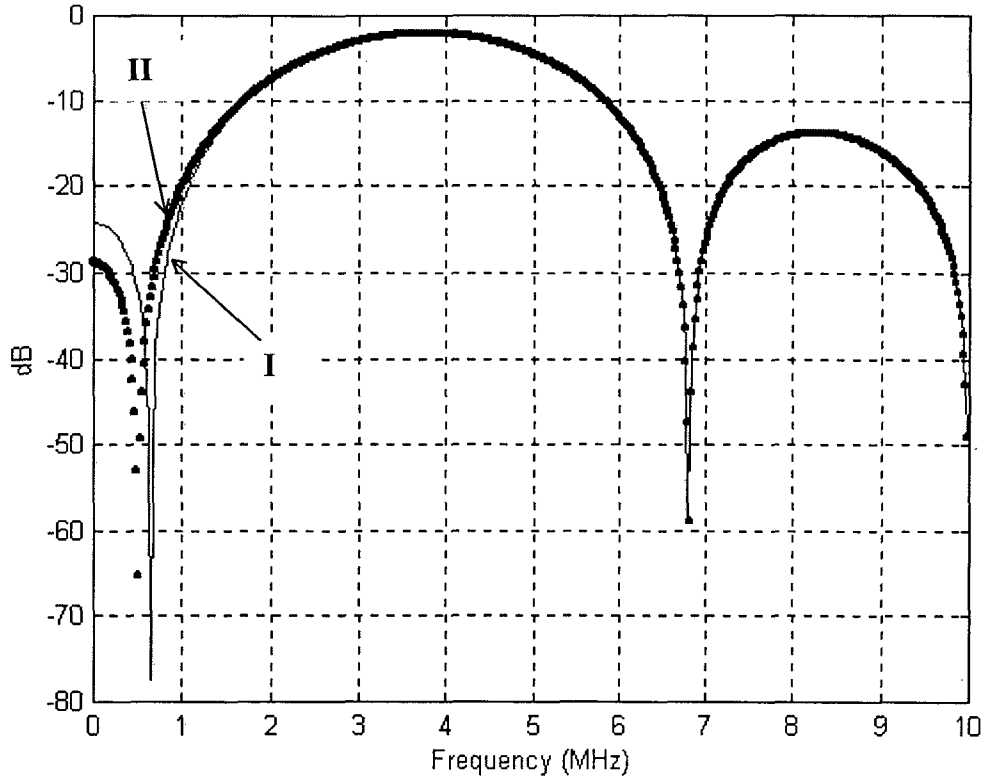


Fig. 5.16 The frequency response of the bandpass filter-II.
(I) Theory and (II) Simulation.

CHAPTER 6

FILTER LAYOUT AND TESTING

6.1 INTRODUCTION

The layout art is one important step in silicon implementation. Many circuits such as switched-capacitor and switched-current are analog circuits but digital circuits control them. Recently, analog and digital circuits have been fabricated on the same chip, resulting in a mixed-analog-digital IC chip. The mix of analog and digital generates several problems for circuit designers.

This chapter includes a short brief about the obstacles concerning the layout of mixed analog-digital chips. Layout guidelines are described to reduce coupling between the analog and digital parts. A short paragraph about CAD tools is written. Finally, a description of the layout of some circuits designed during the preparation of this work together with experimental results is presented.

6.2 CONSIDERATIONS ON LAYOUT FOR ANALOG CIRCUITS

Generally, analog integrated circuits suffer from mismatch between circuit elements. Also, any noise coupled to the analog circuit will be processed like an input signal. Mismatch is caused by process variation such as the non-uniform temperature distribution in furnace during wafer processing. All process parameters, for example oxide thickness or doping implant diffusion are dependent of temperature. Moreover, there are other error sources during the photolithography processing and etching. All these errors cause the performance of the integrated circuit to differ from the ideal one.

For example, the offset of op-amps, an important parameter for analog circuit design, must be as low as possible. The offset voltage has two components, the random offset and the systematic offset. The first one is caused by random mismatch while the second one is caused by asymmetry in circuit configuration. The circuit layout must try to minimize the effects of mismatch by using common centroid layout or trimming techniques [61]. To improve matching, several layout design guidelines have been collected in [63-chpt. 6, 64-chpt. 16].

One of the analog layouts for CMOS cells is the stacked layout method [64, 65]. In this method, the large W/L ratio of the designed transistor is implemented as n elementary transistors connected in parallel, as shown in Fig. 6.1 (c).

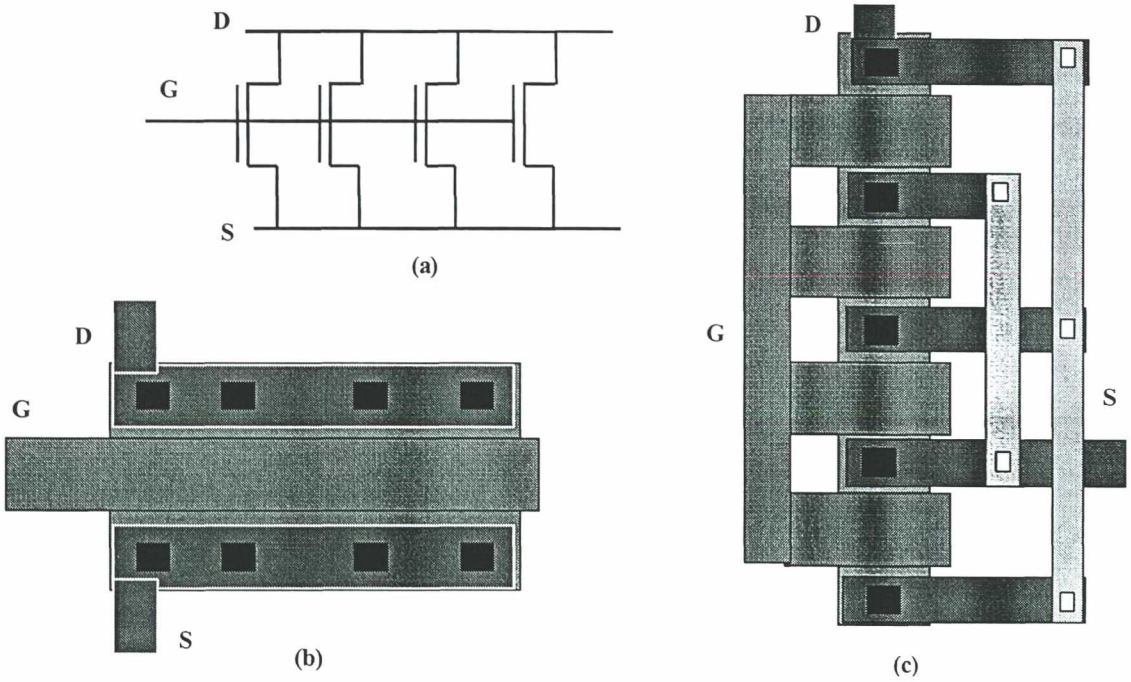


Fig. 6.1. Different layouts for wide MOS transistors.

(a) Transistor schematic.

(b) Layout of a single MOST.

(c) Layout using stack method.

The source and the drain of two-adjacent transistors are overlapped; thus, the overall area is smaller and the parasitic capacitor C_{sb} and C_{db} are reduced by the same factors, which is quite important for high-speed applications. With shrinking process geometry ($L<2\mu m$), boundary effects are becoming more important due to fringing or anisotropic photo-lithographic processing. Dummy elements have been used to match boundary effects [65].

6.3 CONSIDERATIONS ON LAYOUT FOR MIXED ANALOG-DIGITAL CHIPS

In addition to mismatch, mixed analog-digital IC chips suffer from noise coupling (cross-talk) between analog and digital circuits. For example, in the circulating SI analog FIR filter presented here, the digital control circuit that rotates the FIR coefficients generates digital switching noise that can degrade the performance of the filter. As regards layout, the most obvious solution to avoid digital noise to interact with the analog section is a reasonable distance between the digital and analog parts of the chip. An appropriate floor plan for mixed chips is shown in Fig. 6.2. In the mixed chip, there are different ways for the noise to be coupled between the chip parts (analog and digital). The most significant part of the noise is coupled through the common power supply line and into the substrate. Also the noise can be coupled into the signal lines. Some important guidelines that were utilized in our design to reduce noise coupling, are

1- Separate routing for analog and digital power supply (digital and analog power supplies are separated and tied only at a common pad).

2- Guard rings around digital part have been designed (n-well guard ring connected to V_{DD} and P^+ ring connected to V_{SS}).

3- The sensitive circuit parts such as capacitors are shielded.

4- Bottom-plates of the capacitors are connected to op-amp outputs.

More details about layout guidelines can be found in [62-chpt.6, 63-chpt.16]

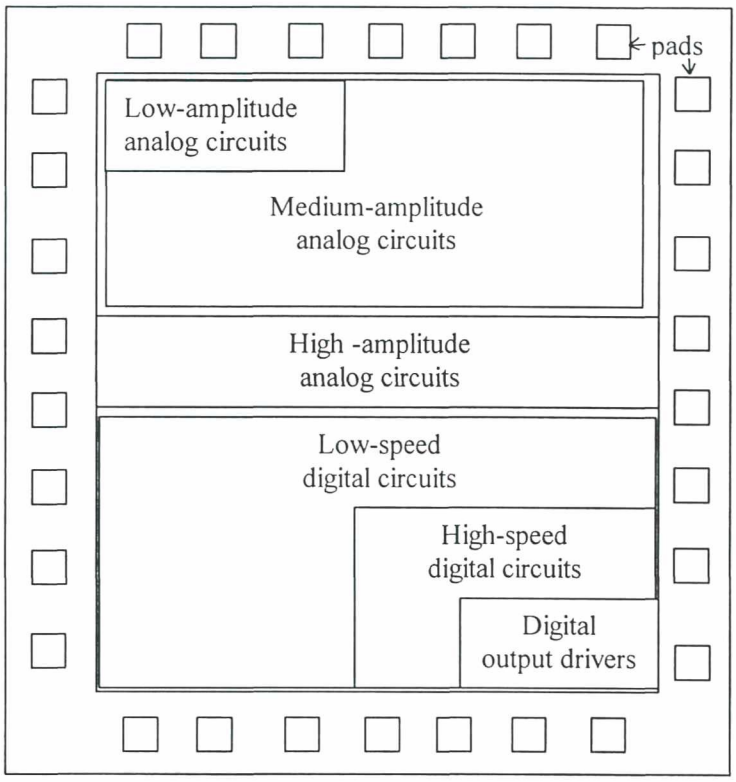


Fig. 6.2. General floor plan for mixed analog-digital chip [62-chpt. 6].

6.4 CAD TOOLS[1]

We used the TANNER TOOLS package [49] to assist us in designing the integrated circuits. The Tanner tools system consists of simulation, front-end and netlist, and mask-level simulation.

The simulation part includes an analog/digital simulator (T-Spice), a gate-level simulator, a waveform viewer (W-Edit) and a 3-D finite element thermal analyzer (L-Edit/Therm).

The front-end and netlist tools include a schematic editor (S-Edit) which can generate netlists for use with the gate-level simulator, T-Spice, and L-Edit/SPR (place and route tool). Another existing tool is the layout-versus-schematic (LVS). This program allows comparing an exported netlist from S-edit and an extracted netlist from L-Edit/Extract, or any two Spice file – compatible netlists.

The mask-level tool consists of a layout editor (L-Edit). L-Edit is a graphical mask layout editor. The program includes a unique cross-section viewer that allows the user to simulate grow/deposit, implant/diffusion and etch steps. In addition, the mask-level tool includes an automatic standard cell placement and routing package (L-Edit/SPR), which allows one to generate layouts for standard cells and automatically construct entire chips. The program accepts the netlists of S-Edit and creates masks ready for fabrication.

L-Edit/Extract generates Spice-compatible circuits netlists from the mask-level layout. It can recognize active, passive devices files and most common device parameters. The extracted file can be easily simulated by T-Spice and the layout-versus-schematic can be readily checked.

Finally, the package includes a design rule check (DRC) routine that can test the designed layout file according to the technology rules. The program allows checking minimum width, exact width, minimum space between the layers, overlap, surroundings, etc. The DRC can handle full chip or part of it.

The program supports three output formats. The program can handle Tanner Database (TDB), Caltech intermediate form (CIF) and GDS II format files.

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[1] Some parts of this section have been transcribed from the user manual of the Tanner tools.

6.5 LAYOUT OF THE SINGLE-ENDED 4-TAP FIR FILTER

The 4-tap switched-current filter designed in chapter 5 has been laid out using L-Edit. The stacked layout technique [64, 65] has been used for the analog circuits. The digital circuit has been designed using standard cells of AMS. Layout guidelines have been taken into account to minimize the coupling between sections. The common centroid technique has been applied in the analog circuit to reduce mismatch effects, especially in differential pairs of op-amps, as shown in Fig. 6.3.

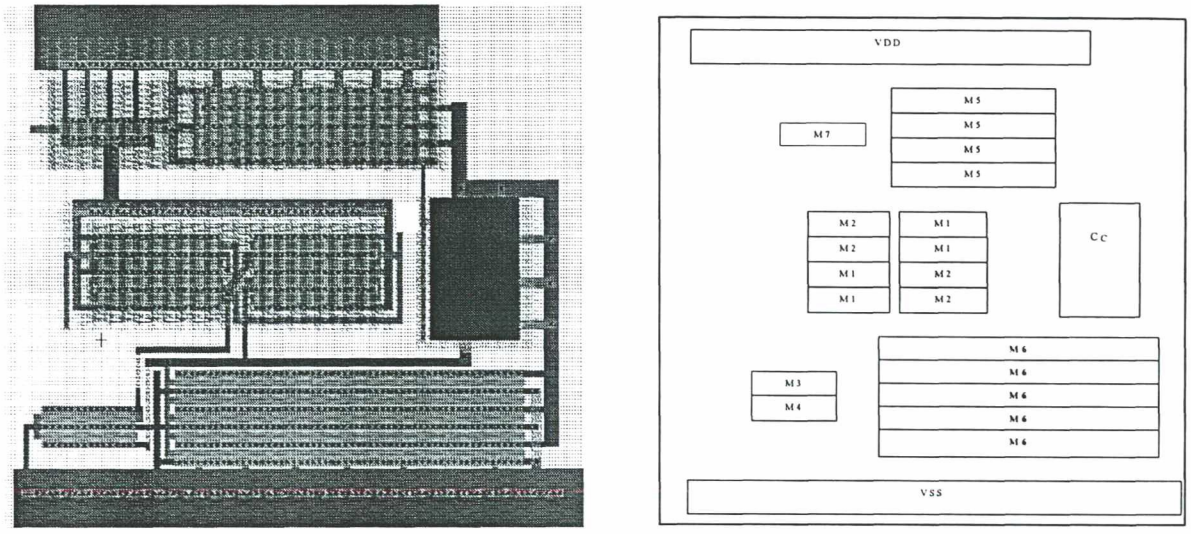


Fig 6.3. Op-amp layout (see schematic in Fig. B.1).

The complete layout of the test chip is illustrated in Fig. 6.4. (a). In this figure, h_1, h_2, h_3, and h_4 are 6-bit digital words for the MOCDs that perform as the FIR filter coefficients. Fig. 6.4. (b) exhibits the floor plan of the chip. The circuit occupies $4mm^2$ die area with pads. The chip has been designed and fabricated in the 0.8μm CMOS technology from AMS.

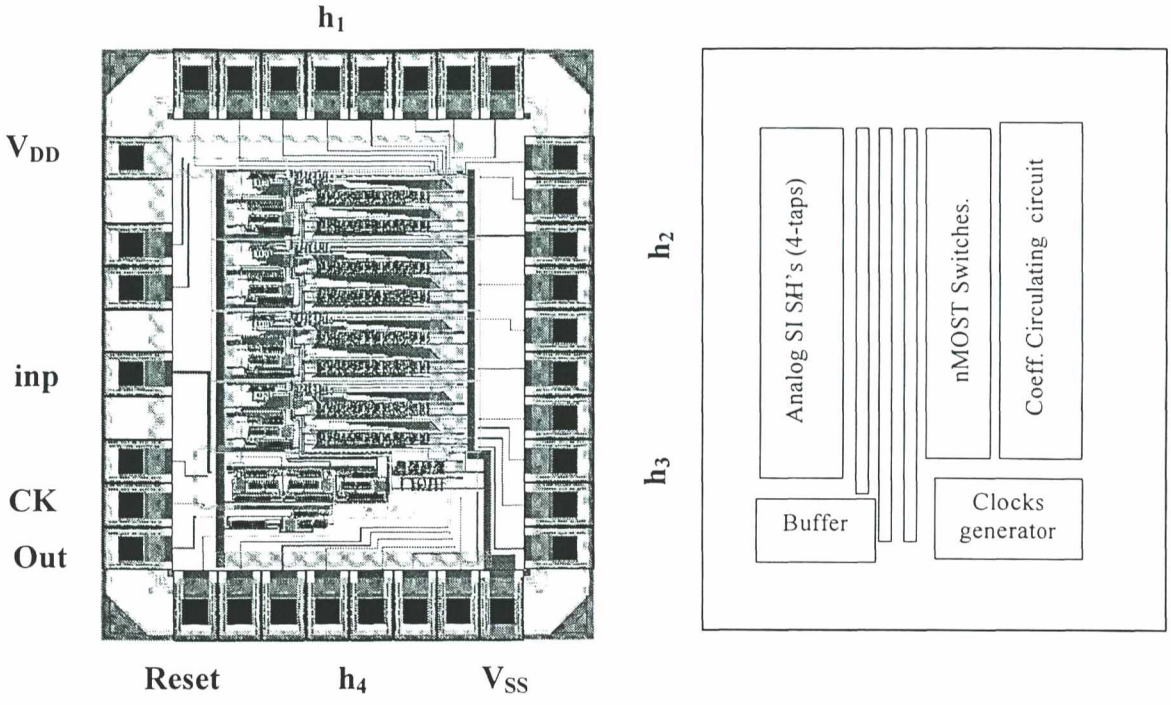


Fig. 6.4. The layout of the single-ended 4-tap FIR filter.

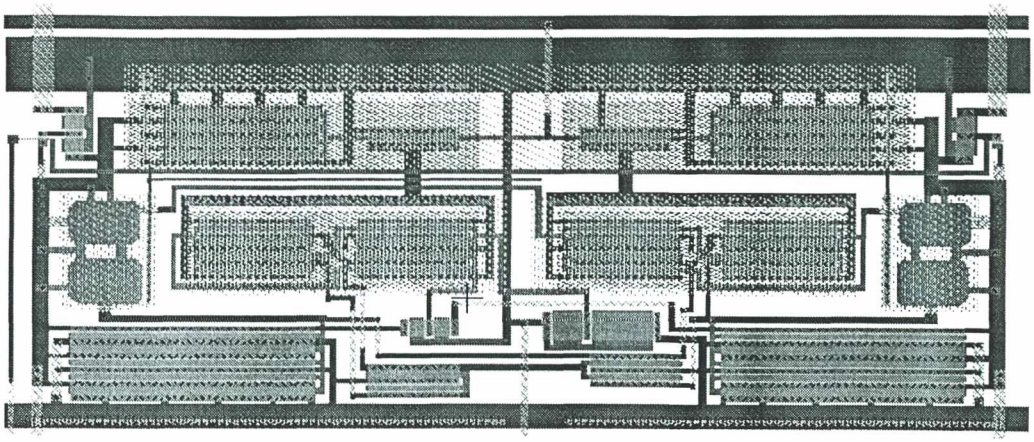
(a) Chip layout.

(b) Floor plan.

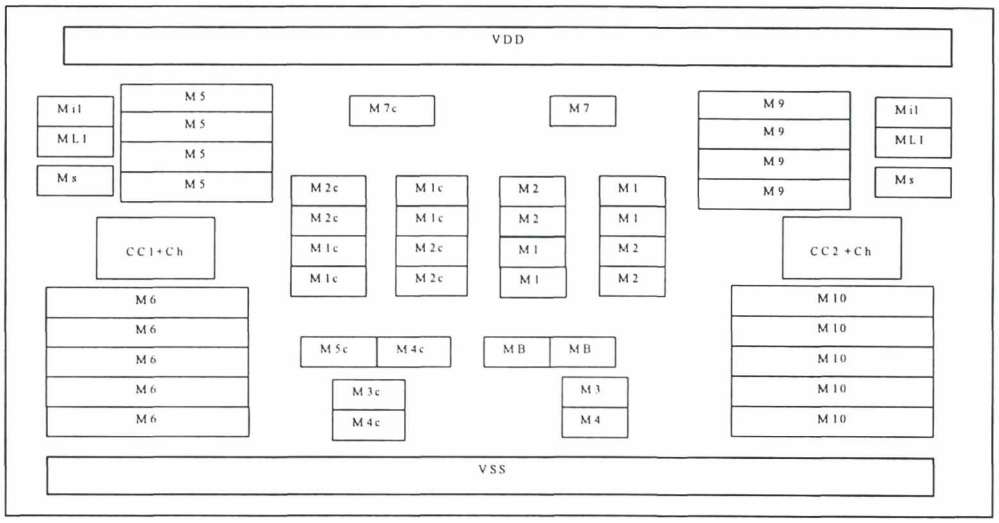
6.6 LAYOUT OF THE FULLY BALANCED SAMPLE-HOLD

The layout of the fully balanced S/H is shown in Fig. 6.5. The layout of the test chip is shown in Fig. 6.6 (a). The total area is 3.5mm^2 including the pads. The test chip includes a complete programmable tap (V-I converter, full programmable SI S/H and I-V converter sections), fully balanced differential op-amp and single-ended to balanced-output converter section. The digital part [1] includes one shift register to load the digital word in serial form. The circuit has been sent to fabricate in the 0.8μm CMOS technology from AMS. The floor plan of the test chip is shown in Fig. 6.6 (b).

[1] This part of the circuit has been designed by undergraduate student William Prodanov.



(a)



(b)

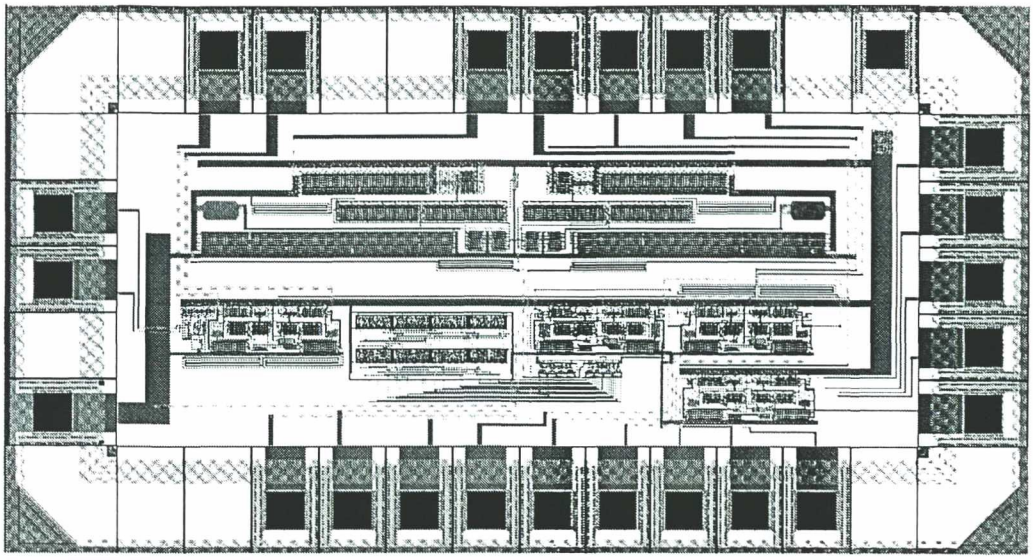
Fig.6.5. Layout of the fully balanced sample-hold and transistor placement.

(a) Layout of the fully balanced S/H.

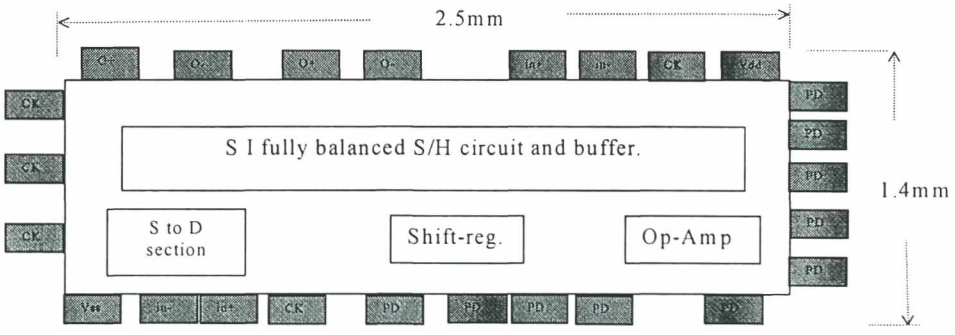
(b) Transistor placement.

6.7 CHIP TESTING AND MEASUREMENTS

A 4-tap switched-current FIR filter was fabricated in the double-poly double-metal 0.8μm CMOS process from AMS. A micrograph of the integrated filter is shown in Fig. 6.7. The entire chip measures 4.0mm^2. Fig. 6.8 shows some details about the single-ended SI S/H circuit.



(a)



(b)

Fig. 6.6. The fully balanced test chip.

(a) Layout of the fully balanced test chip.

(b) Floor plan.

The frequency response has been measured using the 3588A spectrum analyzer. The measured results for different digital words are depicted in Fig. 6.9. The figure shows good agreement between each of the theory, simulation and the experimental results. The time response of the circuit shown in Fig. 6.10 has been obtained for a programmed 4-clock cycle delay.

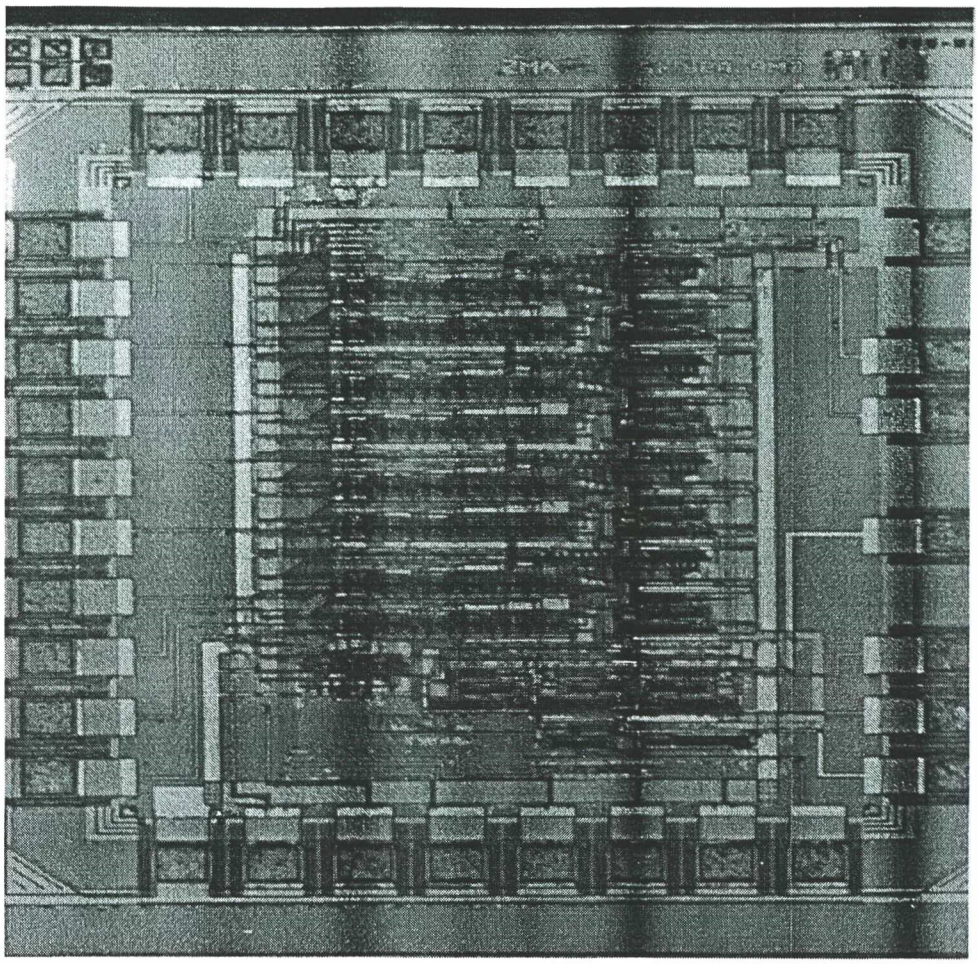
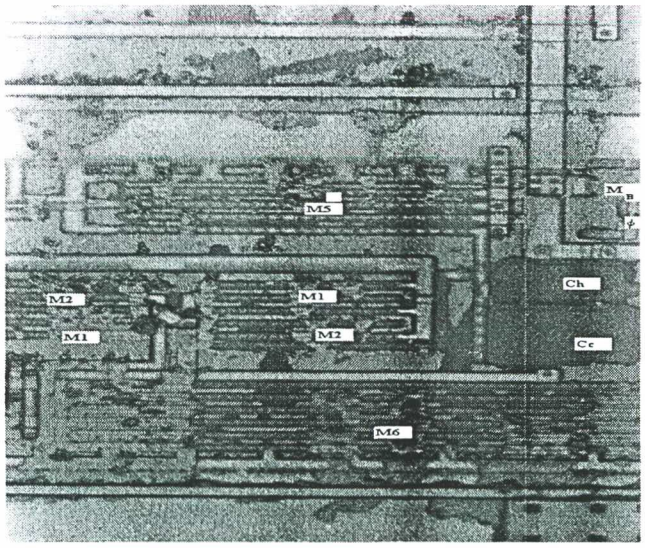


Fig. 6.7 The single-ended 4-tap FIR filter chip micrograph.



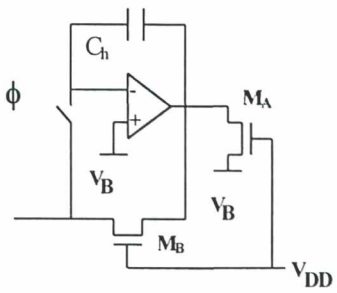
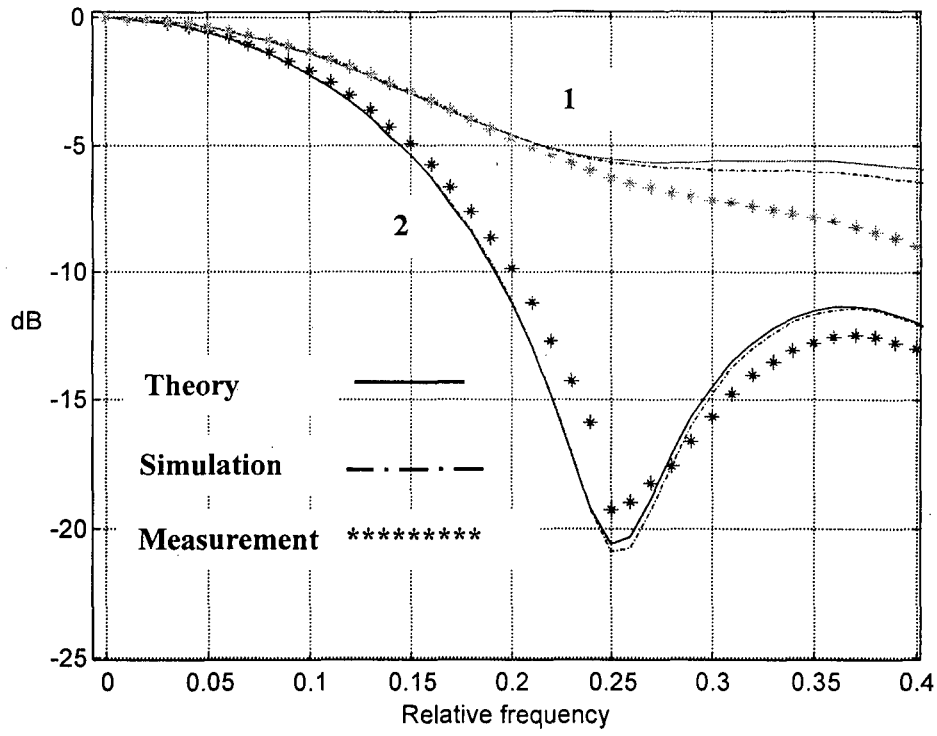


Fig. 6.8 The switched-current S/H.

Obs: M_1, M_2, M_5, M_6 and C_c are the op-amp elements (Fig. B.1).



1 $h_1 = 3F$, $h_2 = 15$, $h_3 = 0B$ *and* $h_4 = 06$.

2 $h_1 = 3F$, $h_2 = 36$, $h_3 = 2E$ *and* $h_4 = 27$.

Fig. 6.9. Measured, simulated and theoretical frequency response of the 4-tap FIR filter.

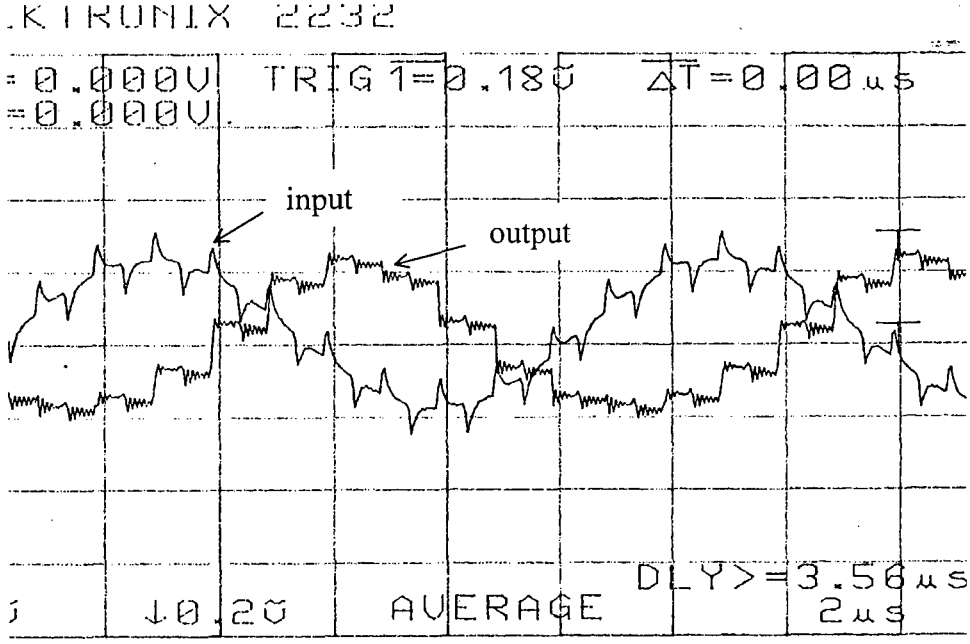


Fig. 6.10. Pure delay measurement.

CONCLUSIONS

In this work, digitally programmable switched-current circuits suitable for low-voltage applications have been proposed. The switches operate at constant voltage avoiding both the "conduction gap" and the signal-dependent charge injection. The programmability of the filters is achieved using the MOSFET only current divider (MOCD). The MOCD's occupy small areas as compared to the conventional SI binary weighted transistors and the capacitor arrays in the SC technique.

A programmable second order section has been implemented. The center frequency and the quality factor of the SI biquad section can be controlled independently.

A programmable SI sample-hold circuit has been designed for 20 MHz sampling frequency applications. A programmable 4-tap FIR filter has been designed and integrated. The circulating technique has been employed for the FIR realization to reduce the offset and re-sampling error accumulation. The test chip has been fabricated in the double-poly double-metal 0.8μm CMOS process from AMS with silicon area 4.0mm^2 and total power 60mW from ± 1.5 power supply.

Also, a fully balanced (FB) programmable switched-current sample-hold circuit has been proposed and integrated for 20 MHz clock frequency. Furthermore, a new methodology for negative sign-bit realization has been proposed and tested. A complete fully balanced SI tap has been designed. The circuit occupies 0.8mm^2 die area. A programmable 8-tap fully balanced FIR filter has been designed using the proposed FB S/H circuit.

APPENDIX A

MOSFET MODEL IN STRONG INVERSION

The basic equation [22] that describes the drain current of the MOS transistor as a function of terminal voltages is

$$I_D = \left(\frac{W}{L}\right)\{f(V_G, V_S) - f(V_G, V_D)\} \quad (A.1)$$

where W is the channel width, L is the channel length and the V_G,V_S, and V_D are gate, source, and drain voltages referred to the substrate, as illustrated in Fig. A.1.

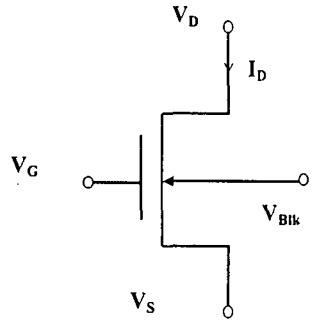


Fig. A.1. NMOS transistor.

In this work, the NMOS transistors in the current divider operate with gate potential equal to V_{DD}. So, they operate in strong inversion. In strong inversion

$$f(V_G, V_{S(D)}) = \frac{\mu n C'_{ox}}{2}\{V_p(V_G) - V_{S(D)}\}^2 \quad (A.2)$$

where V_P (V_G) is the pinch-off voltage of the MOS transistor, n is the slope factor, μ is the carrier mobility and C'_{OX} is the oxide capacitor per unit area. V_P depends on the gate voltage [30] and can be approximated as

$$V_p = \frac{V_G - V_{TO}}{n} \quad (A.3)$$

The slope factor (n) depends slightly on the gate voltage.

(A.1) can be written as:

$$I_D = (I_F - I_R) = I_S(i_f - i_r) \tag{A.4}$$

where

$$I_S = I_{SQ}\left(\frac{W}{L}\right) \qquad I_{SQ} = \mu nC'_{ox}\frac{\phi_t^2}{2}$$

and $$i_{f(r)} = \frac{I_{F(R)}}{I_S}$$

where I_{SQ} is the normalization current for a square transistor, $I_{F(R)}$ is the forward (reverse) saturation current, Is is the normalization current, $i_{f(r)}$ is forward (reverse) normalized current [66], and ϕ_t is the thermal voltage.

The switch conductance can be expressed as

$$g_{DS} = \frac{\partial I_D}{\partial V_D}\Big|_{V_S = V_B} = \mu nC'_{ox}\frac{W}{L}(V_P - V_B) \tag{A.5}$$

For more details about the MOS transistor modeling and symbols, we refer the reader to reference [67-chpt. 2].

APPENDIX B.

DESIGN OF THE TWO-STAGE CMOS OPERATIONAL AMPLIFIER

B.1 GENERAL BACKGROUND [68, 69]

The configuration of a two-stage CMOS Miller Operational Transconductance Amplifier (OTA) is shown in Fig.B.1. The first stage consists of the differential input stage with p-channel MOS transistors ($M_{1,2}$), the biasing current mirror ($M_{7,8}$) and the nMOST ($M_{3,4}$) active load. The second stage is made up of M_6 as the current driver and M_5 as the active load.

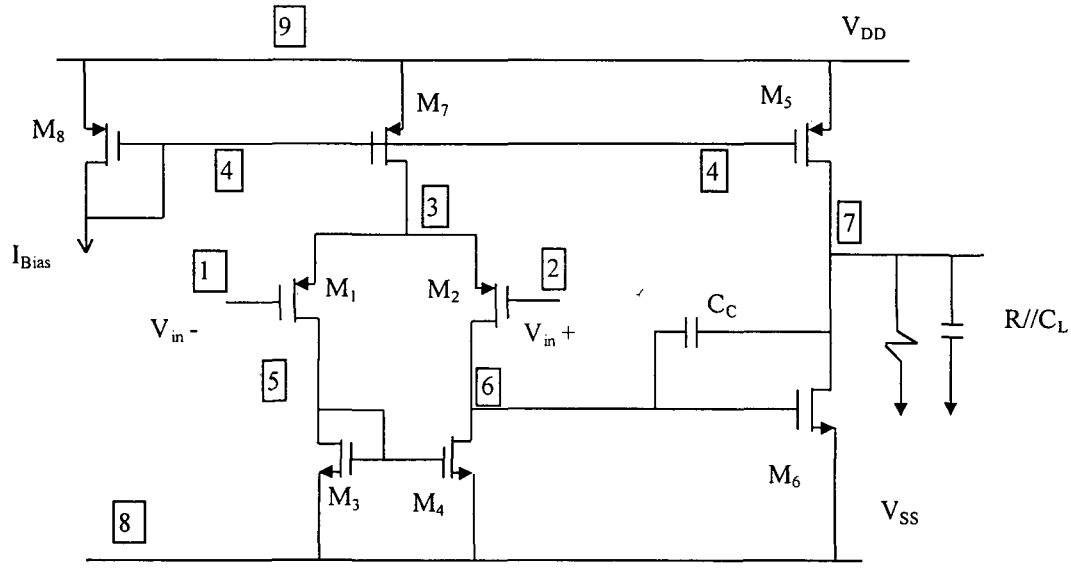


Fig. B.1. Two-stage Miller OTA configuration.

The small signal equivalent circuit is illustrated in Fig. B.2.

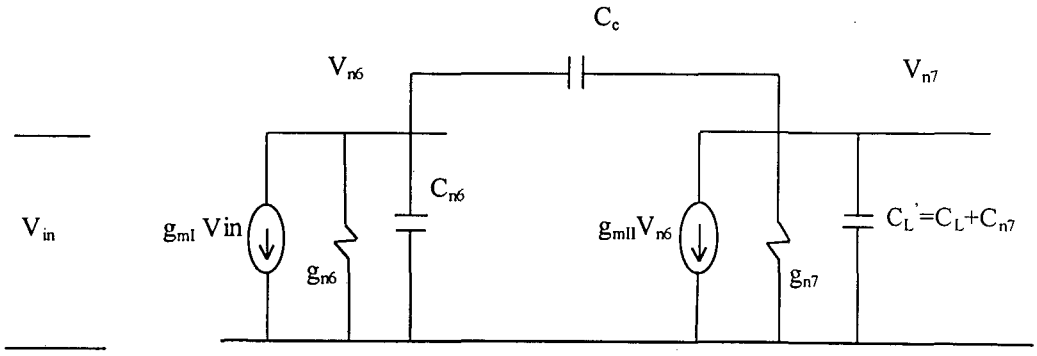


Fig B.2. Small signal equivalent circuit of the amplifier Fig. B.1.

where g_{mI} the transconductance of the first stage (M_1).

g_{mII} the transconductance of the second stage (M_6).

C_{n6} the equivalent parasitic capacitor at node 6.

C_{n7} the equivalent parasitic capacitor at node 7.

g_{n6} the equivalent conductance at node 6 ($g_{d4}+g_{d2}$).

g_{n7} the equivalent conductance at node 7 ($g_{d5}+g_{d6}$).

The basic equations for poles, zero and gain-bandwidth can be written as:

$$f_{p1} = \frac{g_{mI}}{2\pi A_o Cc} \qquad (B.1)$$

$$f_{p2} = \frac{g_{mII}}{2\pi C_L} \qquad (B.2)$$

$$f_z = \frac{g_{mII}}{2\pi Cc} \qquad (B.3)$$

$$GB = \frac{g_{mI}}{2\pi Cc} \qquad (B.4)$$

The DC open loop gain A_o is given by

$$A_o = \frac{g_{mI} g_{mII}}{g_{n6} g_{n7}} \qquad (B.5)$$

The ratio C_c/C_L can be approximated as:

$$\frac{Cc}{C_L} \cong \frac{f_{p2}}{GB} tg(90° - PM) - 1 \qquad (B.6)$$

where PM is the phase margin.

The small circuit parameters (g_{mI}, g_{mII}, C_C) are fully defined if Cc/C_L and f_{p2}/GB are chosen. From the MOS transistor model [22], the aspect ratio (W/L) can be calculated as:

$$\frac{W}{L} = \frac{g_{ms}}{\mu n C'_{ox} \phi_t} \frac{1}{\sqrt{1+i_f} - 1} \tag{B.7}$$

when g_{ms} is source transconductance. More details about the op-amp design methodology are presented in [68, 69]

B.2 OP-AMP DESIGN AND SIMULATION

In the SI technique [21] employed here, the load capacitor of the op-amp is the holding capacitor (C_h) and the parasitic capacitors attached to the output node (C_{n7}). The parasitic capacitors are the gate-drain, overlap and the drain-bulk capacitors of the MOS transistor. The load capacitor is approximated by 2pF. For the sampled–hold circuit designed in chapter 4, the op-amp specifications are presented in Table B.1.

Table B.1: Op-amp specifications.

Parameters of OTA	Values	Dimension
Supply voltage	3(±1.5)	V
Transconductance(g_m).....	~55	mA/V
GB(Gain Bandwidth Product).....	~100	MHz
Phase Margin	>50°	
Load resistance (MOST W=6μm and L=5μm).....	~10	kΩ
Load capacitance (C_L).	2.0	pF

-Design steps

- Select (P_2/GB)=5 → g_{mI}=630 μA/V, g_{mII}=6.3 mA/V and C_C =1pf .

- Select $\gamma = 0.5$.

The geometry of transistors and the simulation results are given in Table B.2. The frequency response and DC transfer function are shown in Fig. B.3.

Table B.2. Design parameters of the op-amp and simulated specifications.

i_{f6}	*300*
i_{f1}	*176*
W of M1,2	*165* μm
W of M3,4	*32* μm
W of M7,8	*32* μm
W of M_5	*300* μm
W of M_6	*600* μm
Total Current	*4* mA
I_{Bais}	*350* μA
GB	*100* MHz
Phase margin	*64°*
A_O	*65* dB

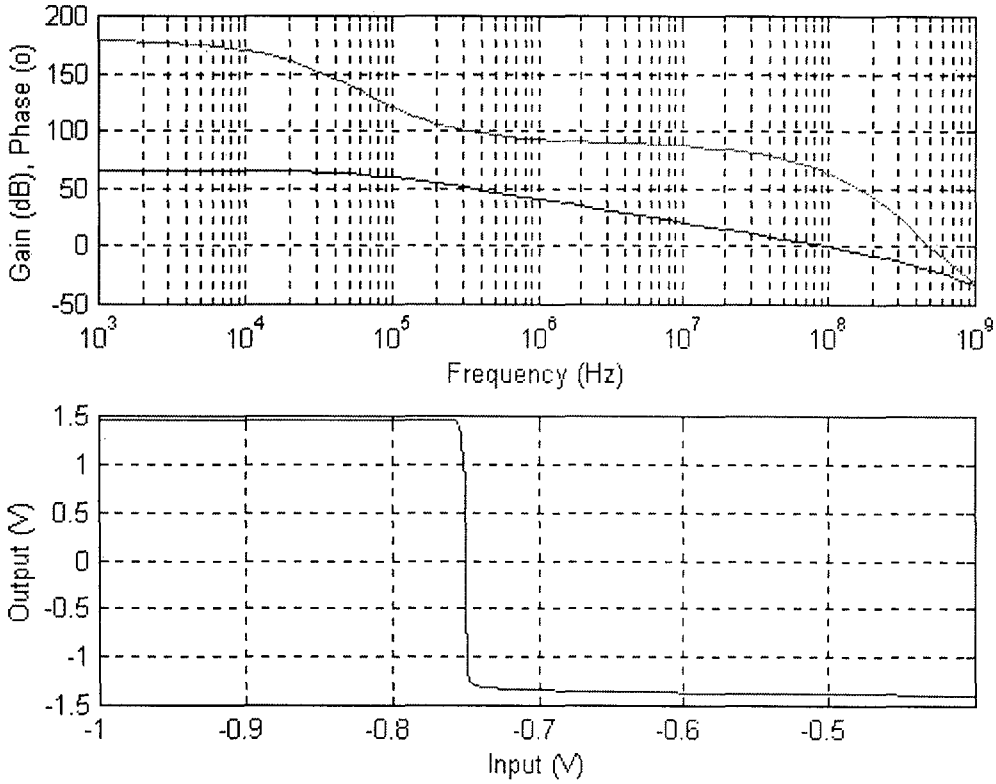


Fig. B.3. The frequency response and the DC transfer characteristic of the op-amp.

To measure the settling time, the op-amp is connected as shown in Fig. B.4. In the simulation result shown in Fig. B.5, the 1% settling time is around 9n sec.

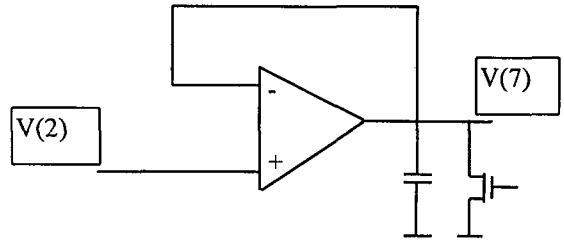


Fig. B.4. Unity gain configuration for measuring the settling time.

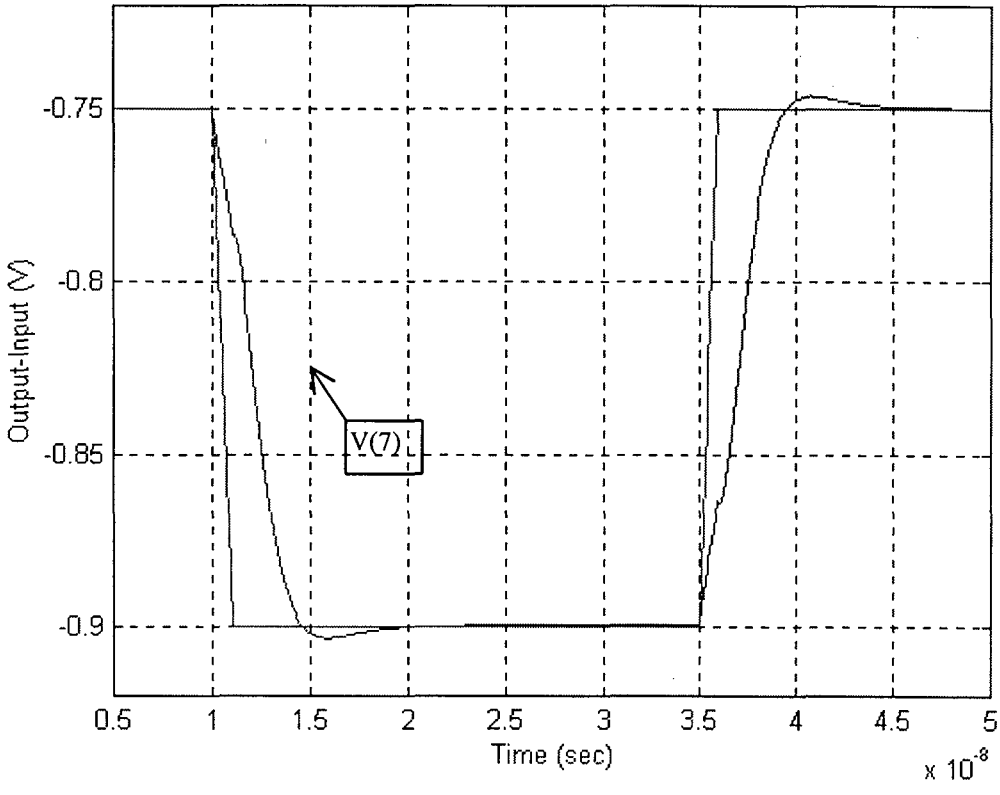


Fig. B.5. The step response of the circuit in Fig. B.4.

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